

Finding Loop Gain in Circuits with Embedded Loops

A Systematic Approach to Multiple-Loop Analysis

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Abstract— *Stability analysis in feedback systems is complicated by non-ideal behavior of circuit elements and by circuit topology. Circuit elements not generally uni-directional transmit a feedforward signal as well as the feedback signal of interest. These signals and node loading must be included in the full analysis. While analysis of single loop designs has been demonstrated to be complete, embedded and multi-loop designs have not been so treated. This paper extends stability analysis to these more general designs using Driving Point Impedance and Signal Flow Graphs to find closed form solutions and to define circuit configurations for simulator generation of loop gain factors.*

Keywords—*feedback, stability, phase margin, embedded loop, driving point impedance, signal flow graph, dpi/sfg*

I. INTRODUCTION

Feedback systems are generally analyzed following H. Black's description based on ideal non-loading and uni-directional blocks¹, Figure 1.

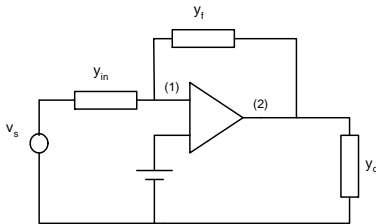


Figure 1: General Ideal Feedback System

The transfer function for this system is given as:

$$H(s) = \frac{A_o}{1 - fA_o} \quad (1)$$

The function in the denominator $fA_o(s)$ is the system loop gain $LG(s)$. As this function approaches 1 Angle 0 the transfer function increases in magnitude becoming sensitive and possibly unstable. The degree of stability is measured as the phase margin of this function, the angle difference from 0 degrees at magnitude 1.

[1] Black, HS, Stabilized Feedback Amplifiers, Bell System Technical Journal, Vol 13, January 1934.

From an ideal block description it is easy to 'open' the loop, drive one end, and look at the return response as LG. Complexities arise in real circuits where loading and bi-directional nature of circuit elements must be considered. The feedback element in Figure 1 loads both output and input ports of the amplifier and allows a feed-forward as well as a feedback signal to propagate, as does the amplifier. If we simply 'open' the loop we change the impedance environment at some nodes and may not account for some bi-directional signals. The 'open' loop gain approximation to LG is dependent on where the loop is broken and to the extent that the elements differ from ideal behavior, passive as well as active, and how we terminate the loop.

A systematic approach to feedback analysis for single loop systems using driving point impedance and signal flow graphs, dpi/sfg², has previously been demonstrated. In this paper we extend this approach to include multiple loop configurations. Section II shows that what may seem like a proper loop gain function extracted from a signal flow graph may be incorrect and we identify the proper loop gain. In section III we show that the proper loop gain function can be obtained from a node impedance analysis. In Section IV, a simulation test bench setup for obtaining loop gain factors is presented and in Section V the process is demonstrated in the analysis of a common mode feedback loop. We conclude and summarize in Section VI.

II. MULTIPLE LOOP FEEDBACK—THE PROPER LOOP GAIN

Consider the two amp embedded feedback configuration shown in Figure 2. Stage 2 has local compensation producing an internal loop embedded in the major loop that contains both amplifiers, a voltage regulator topology.

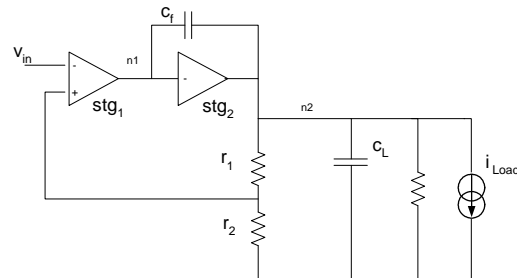


Figure 2: Two Amp Internally Compensated System

[2] Ochoa, A., Analyzing Feedback: Properly Simulating the Open Loop, MidWest Symposium on Circuits and Systems, 1998.

A signal flow graph for this topology is shown in Figure 3 (using simplified amp model parameters— g_{m1} , g_{o1} , etc.). We can ‘solve’ the graph for the system transfer function in the form of (1) by first collapsing the inner loop and identify a potential ‘loop gain’ function LG_1 as (2):

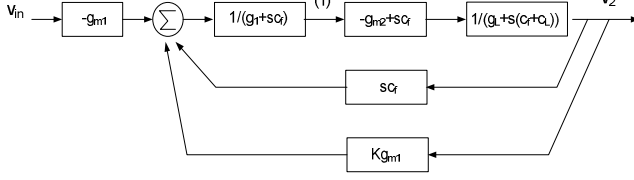


Figure 3: Flow Graph for the Two Amplifier Internally Compensated Loop

$$LG_1 = \frac{\frac{r_i(-g_{m2})}{1+sr_i c_f} \left(1 - \frac{sc_f}{g_{m2}}\right) \frac{r_L}{1+sr_L(c_L+c_f)}}{1 - sc_f \frac{r_i(-g_{m2})}{1+sr_i c_f} \left(1 - \frac{sc_f}{g_{m2}}\right) \frac{r_L}{1+sr_L(c_L+c_f)}} (K \cdot g_{m1}) \quad (2)$$

We could instead perform different graph algebra first transforming this graph into an ‘equivalent’ one before solving the graph. Consider for example combining the two feedback paths into one block containing the sum of the original feedback paths, ($Kg_{m1}+sc_f$). This leads to a different function that can be identified potentially as the system ‘LG’, LG_2 shown in (3).

$$LG_2 = \frac{r_i(-g_{m2})}{1+sr_i c_f} \left(1 - \frac{sc_f}{g_{m2}}\right) \frac{r_L(K \cdot g_{m1} + sc_f)}{1+sr_L(c_L+c_f)} \quad (3)$$

These and other variants can be better seen using a simplified algebra by grouping the blocks in the direct path as ‘A’ and renaming the two feedback paths ‘B’ for ‘ sc_f ’ and ‘C’ for ‘ Kg_{m1} ’.

The combined feedback of ‘B+C’ form results in transfer function:

$$H_{combined}(s) = \frac{A}{1 - A(B+C)} \quad (4)$$

The function subtracted from one in the denominator becomes the potential loop gain function. The ‘collapse of the inner loop first’ transfer relation is:

$$H_{separate}(s) = \frac{A}{1 - AB} \quad (5)$$

$$1 - C \frac{A}{1 - AB}$$

For the graph algebra satisfied with paths ‘B’ and ‘C’ interchanged we obtain yet another form:

$$H_{separate_2}(s) = \frac{A}{1 - AC} \quad (6)$$

$$1 - B \frac{A}{1 - AC}$$

revealing yet another potential loop gain. This pseudo-equivalency is another source of confusion in recognizing the appropriate loop gain function in circuits containing internal loops from signal flow graphs. Graph manipulations result in equivalency only between variables that are not affected by the transformation. Here the input/output transfer function remains constant but internal variables and functional forms that are modified by the transformation do not.

From (4) we see that combining the feedback paths results in the transfer function form that we get from using Mason’s Rule to reduce the algebra of the graph while (5) shows that maintaining the feedback paths separate keeps the pole due to the embedded loop (AB) in the denominator function. The form in (6) confuses the inner loop with the outer feedback path so that the topology grouping is not maintained. Of these results the transfer function in (5) is seen to maintain the circuit grouping as we traverse the outer loop and is the only **proper loop gain**, (2). To find the system loop gain it is necessary to maintain the flow graph in its most primitive form keeping embedded loops closed properly so that they reflect the circuit topology.

III. LOOP GAIN FROM A DRIVING POINT IMPEDANCE ANALYSIS

The driving point impedance of a feedback system is a function of the system loop gain and can be used to extract the proper loop gain. This approach is developed here. First consider a single two port, Figure 4, and its small signal model, Figure 5.

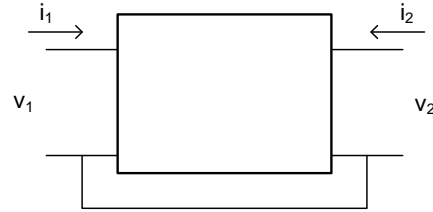


Figure 4: General Two-Port Block

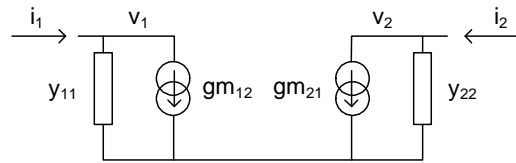


Figure 5: Small Signal y-parameter Model for the General Two Port Block

By shorting input to output we form a feedback system, Figure 6. If we now excite the circuit with a current source we can find the driving point impedance looking into the shorted node as the voltage response. This DPI is a function of a local impedance Z'_x and the system loop gain, (7), from which we find the loop gain to be as given in (8). Since this DPI Z_x is a direct function of the 'proper' loop gain, the function we obtain from the port impedance is the correct loop gain function.

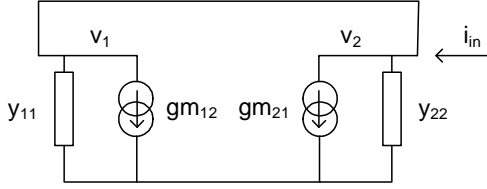


Figure 6: Two Port with Input Shorted to Output

$$Z_x = \frac{Z'_x}{1-LG} = \frac{1}{y_{11} + y_{22} - \frac{1}{1-LG}(-g_{m12} - g_{m21})} \quad (7)$$

$$LG = -\frac{g_{m12} + g_{m21}}{y_{22} + y_{11}} \quad (8)$$

To extend this to an arbitrary circuit as depicted in Figure 7 we first find a wire 'x' in the outer feedback loop and maintain internal loops closed. To find the DPI Z_x we apply a voltage source to node x and split the node as shown in Figure 8. We write for the total input current I_{test} equation (9).

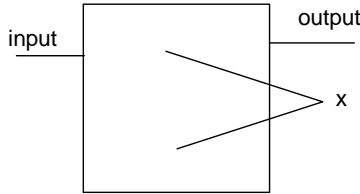


Figure 7: Arbitrary Feedback Circuit with wire 'x' in the Outer Loop.

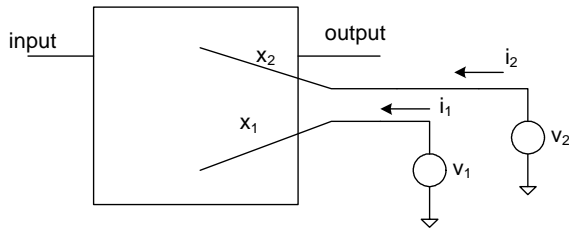


Figure 8: To Find Port Z at 'x' Split the Node and Apply Two Sources.

$$I_{test} = y_{11}v_1 + y_{22}v_2 + y_{12}v_2 + y_{21}v_1 \quad (9)$$

$$I_{test} - (y_{12} + y_{21})v_x = (y_{22} + y_{11})v_x$$

In this last form we separate the input admittance components 'to gnd' from 'cross-coupled' transconductance type. A flow graph for this relation is shown in Figure 9.

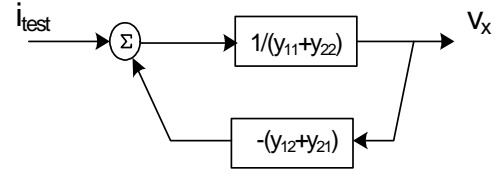


Figure 9: Flow Graph for Port Impedance Z_x

From this graph the loop gain is seen as the product of the two blocks in the loop. The 'cross' terms y_{12} and y_{21} are functionally equivalent to g_{m12} and g_{m21} in (8). With the driving source set to unit magnitude loop gain LG is seen to be the negative of the sum of the cross currents (g_m 's) divided by the sum of the self-currents (to-gnd).

$$LG = \frac{-(y_{12} + y_{21})v_x}{y_{22} + y_{11}} \quad (10)$$

$$= \frac{-(i_{12} + i_{21})}{i_{22} + i_{11}}$$

$$v_x = 1$$

IV. LOOP GAIN SIMULATION BENCH

Loop Gain factors can be obtained from SPICE simulations directly. We can insert an isolation inductor and port coupling capacitors of large magnitudes as shown in Figure 10 and perform two ac sweeps, one with v_2 zero while sweeping v_1 in frequency and the second with v_1 zeroed sweeping v_2 . These simulations can be done in one run and the response currents combined as defined in (10) using the simulator's calculator or by exporting the response variables to a math engine such as Matlab. i_{xy} is current into node x due to excitation y, a transconductance or 'cross' current, while i_{xx} is current into node x due to excitation at x, a 'to-gnd' current.

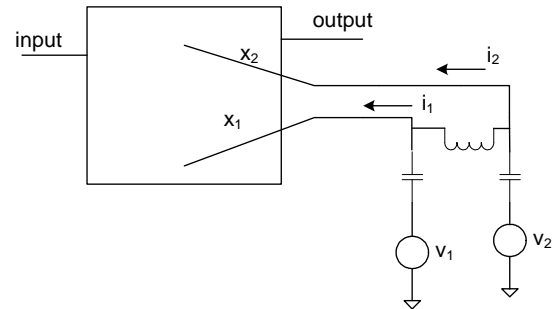


Figure 10: Simulation Coupling of ac Sources to Broken Circuit Node 'x'

V. A COMMON MODE FEEDBACK EXAMPLE

This technique is applied to a common mode feedback loop in a PLL differential loop filter and charge-pump block shown below. The reference current in the pull down charge pump current source nmos diode is corrected by the feedback common mode voltage signal (generated at the loop filter) by a transconductance amplifier driving the voltage at vcm to vref, Figure 11.

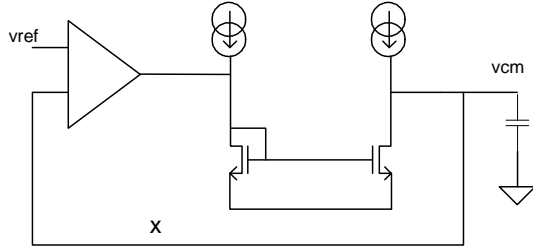
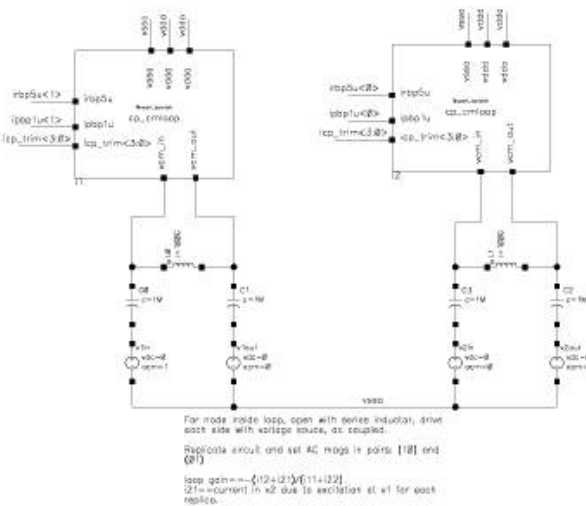


Figure 11: Simulation Setup for a Common Mode Feedback Loop

A top-level test bench for this block is shown in Figure 12. The loop is opened in the outer path at 'x', duplicated and driven as discussed above. The transconductance amplifier is a simple pmos differential stage. The charge pump drives the differential loop filter through a switching network controlled by the phase detector set to short the loop filter terminals for common mode excitation. The common mode voltage v_{cm} is generated from two source follower buffers and resistor summers (not shown). The self and cross currents are combined to create the loop gain function plotted in Figure 13 as magnitude and phase. The loop gain reaches unity at 1MHz



with a phase of 71 degrees.

Figure 12: Simulation Test Bench for Feedback Loop, Charge Pump Common Model

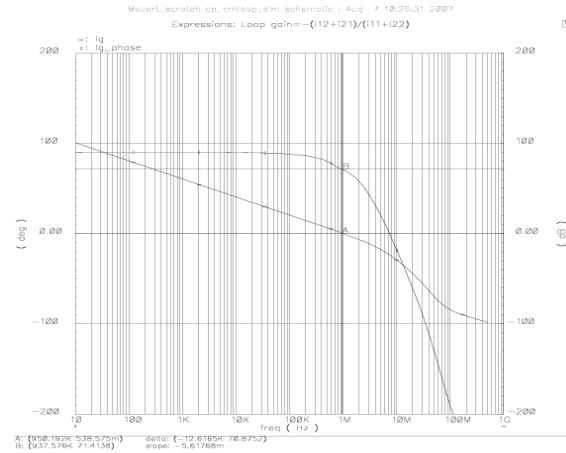


Figure 13: Simulation Response for CP Common Mode Loop Gain, Magnitude and Phase Showing 71 Degrees of Phase Margin

VI. CONCLUSION

System loop gain functions are used to define stability of feedback systems. Obtaining this function is complicated by loading effects, bi-directional transmission in elements, and by circuit topology. A technique using driving point impedance and signal flow graphs has been used previously to find loop gain unambiguously for single loop systems. Multi-loop systems had not been systematically solved for loop gain. In this paper algebra performed on a primitive flow graph for multi-loop systems is shown to generate functions that are not the proper system loop gains—loop gain poles may be cancelled or improper grouping of feedback paths occur changing feedback path associations.

In this paper we have developed the general multi-loop system loop gain from a driving port impedance perspective. Signals generated in a wire in the outer feedback loop are identified as 'self' and 'cross' currents induced to find the driving point impedance at a wire in the outer loop as: ***LG=the negative of the sum of the cross currents (g_m 's) divided by the sum of the self-currents (to- gnd)***. This approach maintains internal loops closed thereby generating the proper loop gain function. A voltage regulator topology is analyzed with this approach to find the loop gain in closed form. Simplified device models were used to keep the algebra tractable.

To fully evaluate system loop gain it is necessary to include complicated device models thereby generating complicated algebra. This full model analysis can be done using a circuit simulator such as SPICE. A simulation bench containing two systems is created to demonstrate the approach to obtain the self and cross currents to find the proper loop gain from one simulation run. This approach is demonstrated using a pll common mode feedback loop.

