Bandgap Voltage and Current Reference Designer

Note: This file is a reduced version (true, but hard to believe since this file is so big) of a more extended version. The reduction is still in progress, so please excuse the current errors.

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Introduction

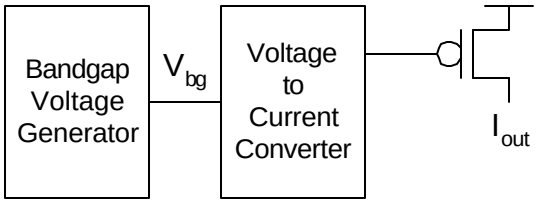


Fig. 0: Overall block diagram of bandgap current generator

A general purpose bandgap voltage generator for BiCMOS technologies is shown in figure 1. Alternate versions of the reference exclude the emitter follower, Q_6, or replace with it with some form of operational amplifier. The emitter follower or operational amplifier circuitry do not contribute much low frequency noise or variance in the output voltage, while migitating second order effects, such as output resistance and base currents. These more advanced versions typically require more area and power, but are usually justified by their advantages. The following design and analysis routines apply the more advanced versions as well.

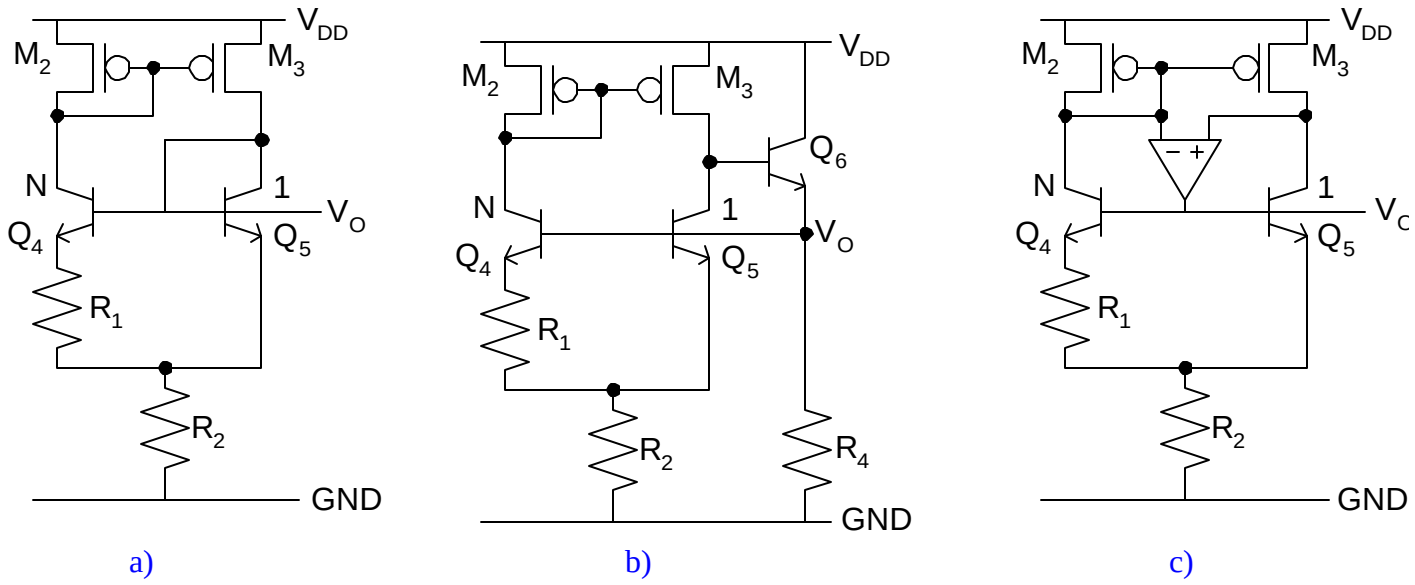


Fig. 1: Basic BiCMOS bandgap circuit with a) no beta-booster,b) emitter-follower beta-booster, and c) op-amp beta-booster.

Almost all reference circuits have multiple stable operating points and require additional start-up circuitry to insure the main circuit is the correct region of operation. The design and sizing of the start-up circuitry is described in a later section. Short channel effects are not added, because the lengths are usually made long for bandgap circuits to improve matching and reduce 1/f noise. The extra length hurts bandwidth, but bandgaps are primarily DC bias circuits, so BW doesn't matter as much.

Inputs

In this section you will enter the requirements for the bandgap, but keep in mind that bandgaps are inherently noisy

Bandgap Voltage:

$V_{DD} := 3V$ **Mean Supply Voltage**

$\sigma_{\Delta Vbg\_Vbg} := 3\%$ **Desired Bandgap 3s Variance**

$v_n := \sqrt{4 \cdot k \cdot Temp \cdot 100k\Omega}$ **Bandgap Noise Density Specification**

$f := 300Hz$ **Frequency for Noise Specification**

Bandgap Current:

$V_{DSsato} := 200mV$ **V_{DSsat} Specification for Output Current**

$f := 300Hz$ **Frequency for Noise Specification**

$I_o := 16\mu A$ **Output Current**

$$4 \cdot 4 \cdot k \cdot Temp \cdot \frac{2}{3} \cdot \frac{2 \cdot I_o}{V_{DSsato}}$$

$$\sigma_{Ion} := \sqrt{4 \cdot 4 \cdot k \cdot Temp \cdot \frac{2}{3} \cdot \frac{2 \cdot I_o}{V_{DSsato}}}$$ **Output Current Noise Specification**

Inputs

Model File

optimal current derivation

General Bandgap Notes

General Bandgap Notes

Bandgap voltages are temperature independent voltages, created by adding the positive temperature coefficient of a thermal voltage to the negative temperature coefficient.

$V_o = V_{BE} + K_{ptat} \cdot V_T = V_{bg}$ Bandgap Output Voltage

The thermal voltage can be expressed as a fixed voltage at the nominal temperature, Temp, rimes normalized temperature:

$$V_T = \frac{k \cdot Temp}{q} \cdot \frac{T}{Temp} \qquad V_{T0} = \frac{k \cdot Temp}{q}$$

The base-emitter voltage can be expressed in the following form. It initially appears to have a positive temperature coefficient, because of the VT term, but the temperature coefficient of I_s will make the overall temperature coefficient of V_{BE} negative.

$$V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right) = V_{T0} \cdot \frac{T}{Temp} \cdot \ln\left(\frac{I_C}{I_S}\right)$$ Base Emitter Voltage

The bias current for the base emitter junction current is usually generated with a PTAT voltage and a resistor. The overall temperature coefficient is found with a combination of the two temperature coefficients.

$$I_C = \frac{V_T}{R(T)} = I_0 \cdot \left(\frac{T}{T_0}\right)^{\alpha}$$ for PTAT current biasing (includes resistor temperature coefficient)

The resistor temperature coefficient is typically around 1000-2000ppm/C for well resistors and +/-300ppm/C for polysilicon resistors.

$R(T) = R_0 \cdot \left[1 + RTC \cdot (T - T_0)\right]$ $RTC := 2070 \frac{ppm}{degC}$ $RTC \cdot Temp = 0.64$

To solve for α, we substitute can make use approximation $(1 + x)^{\alpha} = 1 + \alpha \cdot x$ on R(T)

Ba

$$R_0\cdot\left(\frac{T}{T_0}\right)^{\alpha_R} = R_0\cdot\left(1+\frac{T-T_0}{T_0}\right)^{\alpha_R} = R_0\cdot\left(1+\alpha_R\cdot\frac{T-T_0}{T_0}\right) = R_0\cdot\left[1+RTC\cdot(T-T_0)\right]$$

$$\alpha_R = RTC\cdot T_0$$

$$I_C = \frac{V_{T0}}{R_0}\cdot\left(\frac{T}{T_0}\right)^{1-\alpha_R} = I_{C0}\cdot\left(\frac{T}{T_0}\right)^{1-RTC\cdot T_0}$$

$\alpha := 1 - RTC\cdot Temp \qquad \alpha = 0.36$ Current Source Temperature Coefficient

$$I_S = \frac{q\cdot n_i^2\cdot D_n\cdot A_{EB}}{Q_B}$$ Diode Reverse Saturation Current

$$D_n = V_T\cdot\mu_N = V_{T0}\cdot\frac{T}{T_0}\cdot\mu_N$$ Electron Diffusion Constant

$\mu_N = C\cdot T^{-n} = C\cdot T_0^{-n}\cdot\left(\frac{T}{T_0}\right)^{-n} \qquad n := 0.8$ Electron Mobility as a function of Temperature

$$n_i^2 = D\cdot T^3\cdot e^{\frac{-V_{G0}}{V_T}} = D\cdot T_0^3\cdot\left(\frac{T}{T_0}\right)^3\cdot e^{\frac{-V_{G0}\cdot T_0}{V_{T0}\cdot T}}$$ Instrinsic Carrier Concentration as a function of Temperature

Making substitutions for n_i^2, m_N, D_n, I_S and I_C into V_{BE} then simplifying yields:

$$V_{BE} = V_{G0} - V_T\cdot\left[(4-n-\alpha)\cdot\ln(T) - \ln\left[\frac{Q_B\cdot I_0\cdot\left(\frac{1}{T_0}\right)^{\alpha}}{D\cdot k\cdot C\cdot A_{EB}}\right]\right] = V_{G0} - V_{T0}\cdot\frac{T}{T_0}\cdot\left[(\gamma-\alpha)\cdot\ln\left(\frac{T}{T_0}\right) + \ln\left(\frac{I_0\cdot Q_B}{q\cdot D\cdot V_{T0}\cdot C\cdot T_0^{3-n}\cdot A_{EB}}\right)\right]$$

Making the following substitutions

$$EG = \frac{I_0\cdot Q_B}{q\cdot D\cdot V_{T0}\cdot C\cdot T_0^{3-n}\cdot A_{EB}} \qquad \gamma := 4-n$$

Yields the following results

$$V_{BE} = V_{G0} - V_T\cdot\left[(\gamma-\alpha)\cdot\ln\left(\frac{T}{T_0}\right) - \ln(EG)\right]$$

Making substitution for V_{BE} into V_o.

$$V_o = K_{ptat}\cdot V_{T0}\cdot\frac{T}{T_0} + V_{G0} - V_{T0}\cdot\frac{T}{T_0}\cdot\left[(\gamma-\alpha)\cdot\ln\left(\frac{T}{T_0}\right) - \ln(EG)\right]$$

Take the derivative of V_o with respect to temperature and set it equal to zero to solve for K_{ptat}:

$$\frac{d}{dT}V_o = 0 = K_{ptat}\cdot\frac{V_{T0}}{T_0} - \frac{V_{T0}}{T_0}\cdot\left[(\gamma-\alpha)\cdot\ln\left(\frac{T}{T_0}\right) - \ln(EG)\right] - \frac{V_{T0}}{T_0}\cdot(\gamma-\alpha)$$

$$K_{ptat} = \left(1+\ln\left(\frac{T}{T_0}\right)\right)\cdot(\gamma-\alpha) - \ln(EG)$$

at $T=T_0$:

$$K_{ptat} = (\gamma-\alpha) - \ln(EG)$$

Plugging K_{ptat} back into the equation for V_o yields:

$$V_o(T) := V_{G0} + \frac{k\cdot T}{q}\cdot(\gamma-\alpha)\cdot\left(1+\ln\left(\frac{Temp}{T}\right)\right)$$

at $T=T_0$:

$V_t := V_{G0} + \frac{k\cdot Temp}{q}\cdot(\gamma-\alpha) \qquad V_t = 1.2812\,V$ Bandgap voltage at center of temperature range

Ba $V_{bg} := V_{G0} + \frac{k \cdot Temp}{q} \cdot (\gamma - \alpha)$ $V_{bg} = 1.2812\,V$ Bandgap voltage at center of temperature range

Here we don't see dependence of the process variations on the bandgap voltage. This will be shown in the next section.

$V_o(Temp_{min}) = 1.2793\,V$ Bandgap voltage at low end of temperature range

$\Delta V_{start} := \frac{k \cdot Temp}{q} \cdot (\gamma - \alpha) \cdot \left[1 - \frac{Temp_{min}}{Temp} \cdot \left(1 + \ln\left(\frac{Temp}{Temp_{min}}\right)\right)\right]$ $\Delta V_{start} = 1.95\,mV$ Error voltage at low end of temperature range

$V_o(Temp_{max}) = 1.2795\,V$ Bandgap voltage at the high end of the temperature range

$\Delta V_{stop} := \frac{k \cdot Temp}{q} \cdot (\gamma - \alpha) \cdot \left[1 - \frac{Temp_{max}}{Temp} \cdot \left(1 + \ln\left(\frac{Temp}{Temp_{max}}\right)\right)\right]$ $\Delta V_{top} = 1.68\,mV$ Error voltage at high end of temperature range

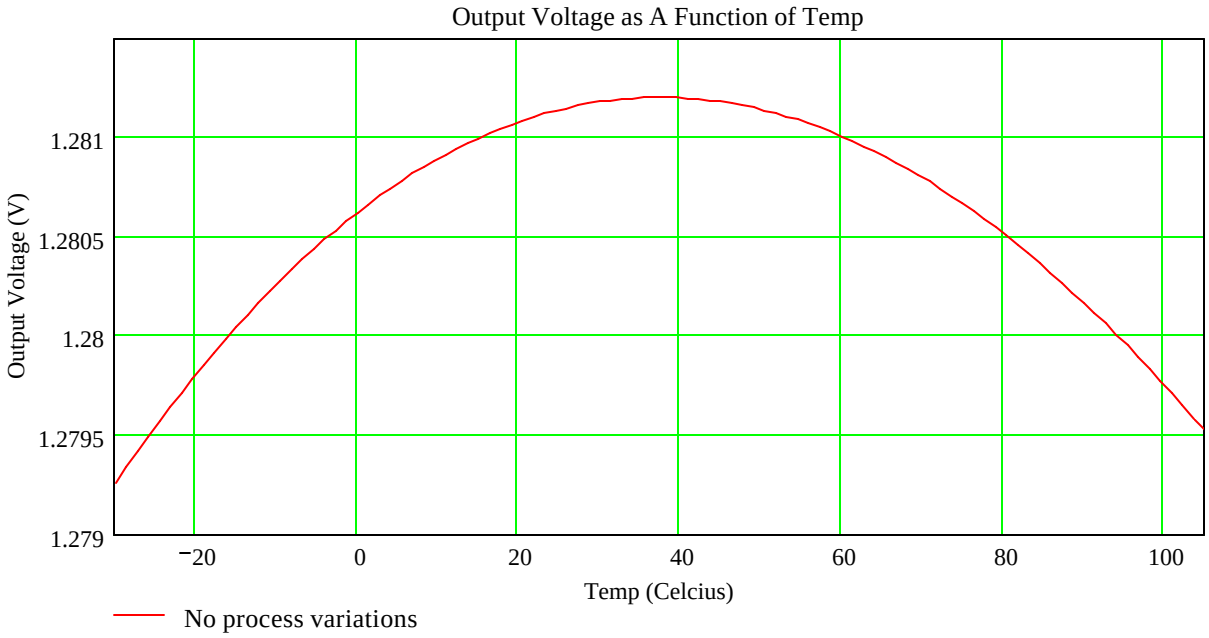
$\Delta V_{max} := \max((\Delta V_{start}\ \ \Delta V_{stop}))$ $\Delta V_{max} = 1.95\,mV$

$V_{ave} := \min((V_o(Temp_{max})\ \ V_o(Temp_{min}))) + \frac{\Delta V_{max}}{2}$ $V_{ave} = 1.28\,V$

$\frac{\Delta V_{max}}{V_{ave}} = 0.15\,\%$ $\frac{\Delta V_{max}}{V_{ave}} = 1.52 \times 10^3\,ppm$ $\frac{\Delta V_{max}}{V_{ave} \cdot Temp} = 4.9\,\frac{ppm}{degC}$

$i := 0..(num - 1)$ Index Vector for Plotting

$TempK_i := \frac{i}{num - 1} \cdot (Temp_{max} - Temp_{min}) + Temp_{min}$ Temperature vector for plotting



Questions and Answers:

Q: What type of resistor should be used to minimize the temperature coefficient of the bandgap voltage?

A: The answer depends on whether the device will be trimmed or not. If it is trimmed than the answer can easily be seen from the equations for DV. If you can make g-a=0, then the bandgap will exhibit no temperature dependence. If you make the substitution for a the equation for DV becomes:

$$\Delta V = \frac{k \cdot T_0}{q} \cdot (\gamma - 1 + RTC \cdot T_0) \cdot \left[1 - \frac{T_{start}}{T_0} \cdot \left(1 + \ln\left(\frac{T_0}{T_{start}}\right)\right)\right]$$

Solving for RTCC, when ΔV is set to zero equals:

$RTC_{opt} := \frac{1 - \gamma}{Temp}$ $RTC_{opt} = -7.09 \times 10^3\,\frac{ppm}{K}$

A negative resistive temperature coefficient of this magnitude is usually not available, so it could be best to use

the most negative temperature coefficient.

Here are some example temperature coefficients from a 0.5um BiCMOS process

$RTC_{NPpoly} := -1150 \frac{ppm}{degC}$ Temperature Coefficient of NP Polysilicon Resistor

$RTC_{PCpoly} := -185 \frac{ppm}{degC}$ Temperature Coefficient of PC Polysilicon Resistor

$RTC_{Nppoly} := 2070 \frac{ppm}{degC}$ Temperature Coefficient of N+ Reach-Through Resistor (diffusion)

$RTC_{NPNbase} := 1350 \frac{ppm}{degC}$ Temperature Coefficient of NPN Base Resistor (diffusion)

$RTC_{NPNEbase} := 2800 \frac{ppm}{degC}$ Temperature Coefficient of NPN Extrinsic Base Resistor (diffusion)

Here are some example temperature coefficients from a 0.5um SiGe BiCMOS process

$RTC_{RIpoly} := -300 \frac{ppm}{degC}$ Temperature Coefficient of Ion Implant Resistor

$RTC_{PBNpoly} := -280 \frac{ppm}{degC}$ Temperature Coefficient of Polysilicon Resistor

Even though the polysilicon resistors will result in a smaller temperature coefficient, the difference between the best and worst ideal temperature coefficients is only 0.7mV, or a 33% reduction in the voltage variance. This difference will more than likely be swamped out by process variations, such as mismatch. The well resistors tend to have less process variations for the same size resistor and area, because their density is higher and they can make their widths wider.

General Bandgap Notes

Basic Bandgap Topology

Basic Bandgap Topology

One of the simplest bandgap and lowest noise bandgap topologies is shown in the following figure. As with all bandgap topologies, it consists a PTAT current generator, which is dropped across a resistor to generate a boosted PTAT voltage. The boosted PTAT voltage is added to the base-emitter voltage of Q1 to realize a bandgap voltage. An advantage of this topology is the bias current for the PTAT generator is shared with the bandgap resistor, R2, which also reduces the required value and noise of R2 by a factor of two.

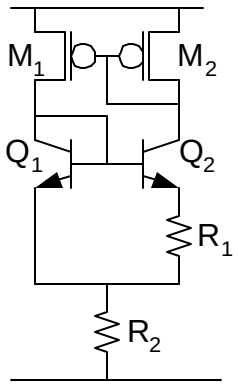


Fig. 1: Basic BiCMOS bandgap with Q1 diode connected.

The disadvantages of this topology in this simplified form, is a weak dependence on power supply voltage, some base current effects, a limitation to a BiCMOS process, and the lack of start-up circuitry. These disadvantages can be overcome with some minor structural changes, which will be explored later in the report.

can be overcome with some minor structural changes, which will be explored later in the report.

When developing bandgap structures a common question arises: "Which side do I diode connect the diode voltages?" Diode connection of either side yields the correct DC value to generate a bandgap voltage, but connection to the resistor side yields an unstable bandgap for this topology. We can see this by looking at the loop gains. The loop gain of the basic bandgap is

$$A_L = \frac{-g_{mQ2}}{1 + g_{mQ2} \cdot R_1} \cdot \frac{1}{g_{mM2}} \cdot -g_{mM2} \cdot \frac{1}{g_{mQ1}} = \frac{1}{1 + g_{mQ2} \cdot R_1}$$

if diode connected around Q_1. If Q_2 is diode connected the loop gain is:

$$A_L = -g_{mQ1} \cdot \frac{1}{g_{mM1}} \cdot -g_{mM2} \cdot \left(\frac{1}{g_{mQ2}} + R_1 \right) = 1 + g_{mQ1} \cdot R_1$$

In both cases we see the loop gain is positive, and thus must be less than one to be stable. We must diode connect Q_1 to make the loop gain less than one to insure stability around the loop.

Basic Bandgap Topology

Bandgap Design Equations

Design Equations

For design, we assume a usage of the basic bandgap topology described above. First, measurure V_{BE} at $T=T_0$, call this $V_{BE0.}$ Using the equations developed above, a value for K_{ptat} can be determined:

$$\ln(EG) = \frac{V_{BE0} - V_{G0}}{V_{T0}}$$

Thus $K_{ptat} = (\gamma - \alpha) - \ln(EG)$ can be simplified to

$$K_{ptat} = \frac{V_{G0} - V_{BE0}}{V_{T0}} + (\gamma - \alpha)$$

Start by with KVL to find the output voltage

$$V_o = V_{BE5} + 2 \cdot I \cdot R_2$$

Subtituting for I: $I = \frac{V_{BE5} - V_{BE4}}{R_1} = \frac{V_T \cdot \ln(N)}{R_1}$

$$V_o = V_{BE5} + 2 \cdot V_T \cdot \ln(N) \cdot \frac{R_2}{R_1}$$

Set this equal to the general purpose bandgap equation, $V_o = V_{BE} + K_{ptat} \cdot V_T$, now

$$K_{ptat} = 2 \cdot \ln(N) \cdot R2\_R1$$

thus for design, where the subscript, 0, implies these numbers are at T_0.

$$R2\_R1 = \frac{K_{ptat}}{2 \cdot \ln(N)} = \frac{\frac{V_{G0} - V_{BE50}}{V_{T0}} + (\gamma - \alpha)}{2 \cdot \ln(N)}$$

Bandgap Design Equations

Headroom Constraints

Bandgap Headroom Constraints

The first step of most device sizing procedures is to define headroom constraints, which often fixes the values

for many V_{DSsat}'s. Here this requires knowledge of the maximum and miminum values for the bandgap voltage.

$V_{bgmax} := V_{bg} \cdot (1 + \sigma_{\Delta Vbg\_Vbg})$ $V_{bgmax} = 1.32\,V$

When sizing the PMOS current mirror for the bandgap it is desirable to make the V_{DSsatP} as large as possible to reduce it's noise contribution to the output. There are two headrom constraints, which limit the size the V_{DSsatP}. The first constraint on V_{DSsatP} is set when the one of the PMOS transistors goes into the linear region.

$V_{DSsatP} := V_{DDmin} - V_{bgmax}$ $V_{DSsatP} = 1.38\,V$

The constraint is to prevent one of the bipolar transistors from going into saturation. This is almost always the tougher constaint as $V_{TPmax}+V_{CEsat}$ is usually greater than V_{BEmin}.

$V_{DSsatP} := V_{DDmin} - V_{TPmax} - V_{bgmax} + V_{BEmin} - V_{CEsat}$ $V_{DSsatP} = 0.78\,V$

If a emitter follower is used to reduce the effects of base current, the V_{DSsatP}'s of the PMOS devices must be reduced

$V_{DSsatP} := \text{if}(\text{BetaHelper} = 1, V_{DDmin} - V_{TPmax} - V_{bgmax} - V_{CEsat}, V_{DSsatP})$ $V_{DSsatP} = 0.78\,V$

Using a minimum desired V_{DSsat} we can determine the minimum supply voltage for this topology:

$V_{DDbgmin} := \text{if}(\text{BetaHelper} = 1, V_{bgmax} + V_{DSsatmin} + V_{CEsat} + V_{TPmax}, V_{bgmax} + V_{DSsatmin} + V_{CEsat} + V_{TPmax} - V_{BEmin})$

$V_{DDbgmin} = 2.12\,V$

Headroom Constraints

BiCMOS Bandgap Noise Analysis

Noise Analysis of BiCMOS Bandgap

When calculating the noise from the bandgap, one must ask what is important: integrated noise or noise amplitude at a given frequency. Usually the answer is integrated noise, but in this case the bandwidth is usually set by another circuit and the noise amplitude by the bandgap circuit. Thus the noise at a given frequency is most important for bandgaps. The next question is which frequency? Bandgaps are usually built with BJT devices, which exhibit 1/f noise corners in the 1kHz range, which is negligible for most applications, and so are dominated by 1/f noise of the current mirror for low frequencies.

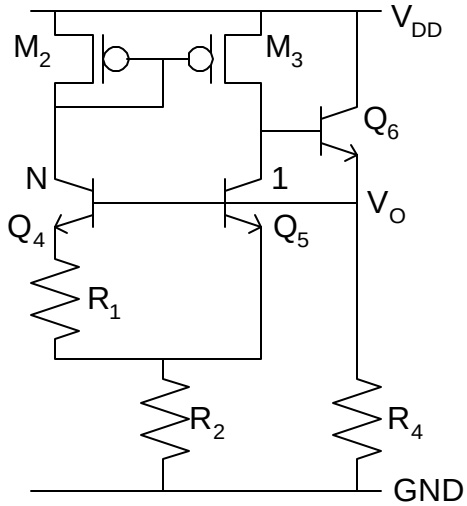


Fig. 1: BiCMOS Bandgap Voltage Circuit

The required noise level for the bandgap can be given directly, or found from a SNDR and BW specification:

$\sigma_{Von} := V_{bg} \cdot 10^{\frac{-SNDR}{20}}$ $\sigma_{Von} = 128.12\,\mu V$ Required Integrated Output Noise

$v_n := \text{if}\left(\text{Find\_vn\_from\_SNDR}, \sqrt{\frac{\sigma_{Von}^2}{BW}}, v_n\right)$ $\quad v_n = 41.44\,\frac{nV}{\sqrt{Hz}}$ Distributed Voltage Noise

There are four equations and four unknowns for the four main nodes of the circuit.

$$v_{G3} = v_{nM3} - g_{mQ3}\cdot\frac{1}{g_{mM3}}\cdot\left(v_{B3} + v_{nQ3}\right)$$

$$v_{B1} = v_{nQ1} + v_{nR1} - g_{mM1}\cdot\left(v_{G3} + v_{nM1}\right)\cdot\left(\frac{1}{g_{mQ1}} + R_1\right)$$

$$v_{B3} = -\left[g_{mM2}\cdot\left(v_{G3} + v_{nM2}\right) + g_{mQ2}\cdot\left(v_{B1} + v_{nQ2}\right)\right]\cdot R_o$$

$$v_{bg} = v_{B1} - g_{mM1}\cdot\left(v_{G3} + v_{nM1}\right)\cdot R_2 + v_{nR2}$$

These equations are simplified to solve for the bandgap voltage

Given

$$v_{G3} = v_{nM3} - \frac{g_{mQ1}}{M}\cdot\frac{M}{g_{mM1}}\cdot\left(v_{B3} + v_{nQ3}\right)$$

$$v_{B1} = v_{nQ1} + v_{nR1} - \frac{g_{mM1}}{g_{mQ1}}\cdot\left(v_{G3} + v_{nM1}\right)\cdot(1 + \ln(N))$$

$$v_{B3} = -\left[g_{mM1}\cdot\left(v_{G3} + v_{nM2}\right) + g_{mQ1}\cdot\left(v_{B1} + v_{nQ2}\right)\right]\cdot R_o$$

$$v_{bg} = v_{B1} - g_{mM1}\cdot\left(v_{G3} + v_{nM1}\right)\cdot R_2 + v_{nR2}$$

$$\text{Find}\left(v_{G3}, v_{B1}, v_{B3}, v_{bg}\right) \rightarrow \left[\begin{array}{l} \\ \\ \\ \\ \dfrac{-R_o\cdot g_{mQ1}^2\cdot v_{nR1} - \ln(8)\cdot v_{nM3}\cdot g_{mM1} - R_o\cdot g_{mQ1}^2\cdot v_{nQ2} - R_o\cdot g_{mQ1}^2\cdot v_{nQ1} + v_{nR2}\cdot g_{mQ1} + R_2\cdot g_m}{} \end{array}\right.$$

$$v_{B1} = \frac{\left(\frac{g_{mM1}}{g_{mQ1}}\right)^2\cdot\left(1 + g_{mQ1}\cdot R_1\right)^2\cdot 2\cdot v_{nM1}^2 + \left[\left(1 + R_1\cdot g_{mQ1}\right)^2 + 1\right]\cdot v_{nQ1}^2 + v_{nR1}^2}{g_{mQ1}^2\cdot R_1^2}$$

$$v_n^2 = \frac{\left(R_2\cdot g_m + 1\right)^2\cdot v_{nR1}^2 + \left(1 + R_2\cdot g_m + \ln(N)\right)^2\cdot v_{nQ2}^2 + \left(R_2\cdot g_m + 1\right)^2\cdot v_{nQ1}^2 + \left(\frac{g_{mM1}}{g_m}\right)^2\cdot\left(1 + R_2\cdot g_m + \ln(N)\right)^2\cdot 2\cdot v_{nM1}^2}{\ln(N)^2} +$$

An important variable is the PTAT coefficient, K_{ptat}:

$$K_{ptat} = \frac{V_{G0} - V_{BE0}}{V_T} + (\gamma - \alpha)$$

$\alpha := 1 - RTC\cdot Temp$ $\quad \alpha = 0.36$ Current Source Temperature Coefficient

$\mu_N = C\cdot T^{-n} = C\cdot T_0^{-n}\cdot\left(\frac{T}{T_0}\right)^{-n}$ $\quad n := 0.8$ Electron Mobility as a function of Temperature

$\gamma := 4 - n$ $\quad \gamma = 3.2$

where V_{BE0} is the diode voltage at the nominal operating temperature, and nominal operating current. a is the

resistor temperature coefficient.

A potential inaccuracy of the design procedure developed here is that K_{ptat} requires a value for V_{BE0}, V_{BE0} requires are value for current, I, and the catch 22 continues with I requiring a value of K_{ptat}. The exact solution involves iteration of the nonlinear equations. To resolve this conflict, we guess at the current to solve for V_{BE0}, and solve for the current. We then recalculate V_{BE0} to find the resistor values. Here we use an initial estimate of I to be 100mA.

$$V_{BE0} := V_T \cdot \ln\left(\frac{100\mu A}{I_s}\right) \qquad V_{BE0} = 0.74\,V$$

$$K_{ptat} := \frac{V_{G0} - V_{BE0}}{V_T} + (\gamma - \alpha) \qquad K_{ptat} = 20.17$$

Making the following substitutions

$$g_{mQ1} = g_m = \frac{I}{V_T} \quad v_{nQ1}^2 = v_{nQ2}^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T}{2 \cdot I} \quad v_{nR1}^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T \cdot \ln(N)}{I} \quad v_{nR2}^2 = 4 \cdot k \cdot Temp \cdot R_2$$

$$R_1 = \frac{V_T \cdot \ln(N)}{I} \qquad g_{mM1} = \frac{2 \cdot I}{V_{DSsatP}} \qquad v_{nM1}^2 = 4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot \frac{2 \cdot I}{V_{DSsat}}} \qquad \frac{R_2}{R_1} = \frac{K_{ptat}}{2 \cdot \ln(N)}$$

$$v_n^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T}{I} \cdot \left[\left(\frac{R_2}{R_1} + \frac{1}{\ln(N)}\right)^2 \cdot \ln(N) + \left(\frac{1}{\ln(N)} + \frac{R_2}{R_1} + 1\right)^2 \cdot \frac{1}{2} + \left(\frac{R_2}{R_1} + \frac{1}{\ln(N)}\right)^2 \cdot \frac{1}{2} + \left(\frac{2 \cdot V_T}{V_{DSsatP}}\right)^2 \cdot \left(\frac{1}{\ln(N)} + \frac{R_2}{R_1} + 1\right)^2\right.$$

Solving for I with assumptions:

$$I := 4 \cdot k \cdot Temp \cdot \frac{V_T}{v_n^2} \cdot \frac{K_{ptat}^2}{2 \cdot \ln(N)} \qquad I = 26.21\,\mu A$$

From the current design equation we see that we want to increase V_{BE0}, to increase K_{ptat}, to reduce the current drain requirements. This means using small transistors. In practice there is a trade-off for device size, as small transistors increase the base resistance and the noise.

Solving for I without assumptions:

$$I := 4 \cdot k \cdot Temp \cdot \frac{V_T}{v_n^2} \cdot \left[\left(\frac{K_{ptat}}{2 \cdot \ln(N)} + \frac{1}{\ln(N)}\right)^2 \cdot \ln(N) + \left(\frac{1}{\ln(N)} + \frac{K_{ptat}}{2 \cdot \ln(N)} + 1\right)^2 \cdot \frac{1}{2} + \left(\frac{K_{ptat}}{2 \cdot \ln(N)} + \frac{1}{\ln(N)}\right)^2 \cdot \frac{1}{2} + \left(\frac{2 \cdot V_T}{V_{DSsatP}}\right)^2 \cdot \left(\frac{1}{\ln(N)}\right.\right.$$

$$I = 36.8\,\mu A$$

A more accurate way of calculating the current involves including the effects of 1/f noise and optimizing for cost, with a lower limit being set by the current required for thermal noise. 1/f noise can be decreased by increasing the device area without affecting current, so it is desirable to make the current as low as possible. Analysis has shown leaving 3dB margin for 1/f and thermal noise is usually close to the value to minimize overall cost.

$$I := if(No1\_f = 1, I, 2 \cdot I) \qquad I = 73.61\,\mu A$$

If I is constrained to a fixed value we replace the calculated current, with the constrained value.

$$I := I_{fix}(I) \qquad I = 73.61\,\mu A$$

Solving for PMOS 1/f noise alone and making variable substitutions:

$$v_{nM1}^2 = \frac{K_{fP}}{W_P \cdot L_P \cdot f} \qquad W_P = \frac{2 \cdot I \cdot L_P}{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}$$

$$v_{bg1\_f}^2 = \left(\frac{2 \cdot V_T}{V_{DSsatP}}\right)^2 \cdot \left(\frac{1}{\ln(N)} + \frac{K_{ptat}}{2 \cdot \ln(N)} + 1\right)^2 \cdot 2 \cdot v_{nM1}^2 = 4 \cdot V_T^2 \cdot \left(\frac{1}{\ln(N)} + \frac{K_{ptat}}{2 \cdot \ln(N)} + 1\right)^2 \cdot \frac{K_{fP} \cdot \mu_P \cdot C_{OX}}{I \cdot L_P^2 \cdot f}$$

Solving for the required length given half of the noise is thermal noise:

Ba $L_{P1\_f} := \sqrt{4 \cdot V_T^2 \cdot \left(\frac{1}{\ln(N)} + \frac{K_{ptat}}{2 \cdot \ln(N)} + 1 \right)} \cdot \frac{K_{fP} \cdot \mu_P \cdot C_{OX}}{I \cdot \frac{v_n^2}{2} \cdot f}$ $L_{P1\_f} = 0.45\,\mu m$

Once the current is known for the bandgap, the resistor values can be found. This requires a recalculation of the K_{ptat} variable.

$V_{BE0} := V_T \cdot \ln\left(\frac{I}{I_s}\right)$ $V_{BE0} = 0.73\,V$

$K_{ptat} := \frac{V_{G0} - V_{BE0}}{V_T} + (\gamma - \alpha)$ $K_{ptat} = 20.47$

$R_1 := \frac{V_T \cdot \ln(N)}{I}$ $R_1 = 0.76\,k\Omega$ Widlar Current Resistor

$R_2 := \frac{K_{ptat}}{2 \cdot \ln(N)} \cdot R_1$ $R_2 = 3.73\,k\Omega$ Common Resistor

BiCMOS Bandgap Noise Analysis

Current Mirror Variance

Current Mirror Variance Derivation

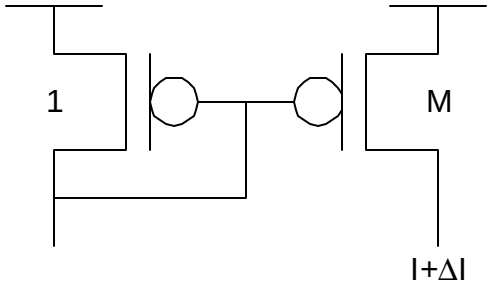


Fig. 1: Current mirror used to find variance

Inputs

$I_{in} := 100\mu A$ **Input Current**

$M := 2$ **Current Mirror Ratio**

$\sigma_{\Delta I\_Ides} := 2\%$ **Matching Requirement**

$V_{DSsat} := 0.3V$ **V_{DSsat} of Current Mirror**

Derivation

Before we calculate the variance in the bandgap, it is useful to find the variance in a weighted current mirror. First we start with a basic MOSFET equation for the diode connected portion of the mirror.

$I_{in} = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$ $I_{out} = M \cdot I_{in} + \Delta I$

$I_{out} := M \cdot I_{in}$ $I_{out} = 200\,\mu A$

Now we write an equation for the output portion of the mirror. Here we add mismatches. The width is multiplied by M, by using M transistors the variance in widths of the transistor add to make the overall variance increase by sqrt(M).

$$I_{out} + \Delta I_{out} = \mu \cdot C_{OX} \cdot \frac{\left(M \cdot W_o + \sqrt{M} \cdot \Delta W\right)}{L + \Delta L} \left(V_{GS} - V_T + \Delta V_T\right)^2$$

These two equations can be combined to find the variance in the output of the current mirror.

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$$\sigma_{\Delta I\_Io}^2 = \frac{2^2\cdot\sigma_{\Delta VT}^2}{V_{DSsat}^2} + \frac{1}{M}\cdot\frac{\sigma_{\Delta W}^2}{(W_o-\Delta W)^2} + \frac{\sigma_{\Delta L}^2}{(L-\Delta L)^2}$$

From this equation it would imply that large V_{DSsat} improves current source matching, but we will see this is not true later. Now W is usually sized given L, V_{DSsat}, and I

$$W_o = \frac{2\cdot I_{out}\cdot(L-\Delta L)}{\mu\cdot C_{OX}\cdot V_{DSsat}^2} + \Delta W$$

Making this substitution yields:

$$\sigma_{\Delta I\_I}^2 = \frac{2^2\cdot\sigma_{\Delta VT}^2}{V_{DSsat}^2} + \frac{\sigma_{\Delta W}^2}{M}\cdot\left[\frac{\mu\cdot C_{OX}\cdot V_{DSsat}^2}{2\cdot I_{out}\cdot(L-\Delta L)}\right]^2 + \frac{\sigma_{\Delta L}^2}{(L-\Delta L)^2}$$

This equation implies current source matching is achieved at an optimal V_{DSsat}. We will see this is also not true because we must also substitute an equation for ΔV_T, which is also a function of L and V_{DSsat}.

$$\sigma_{\Delta VTP}(L) = 3\cdot\left[\frac{\sigma_{VTPLmin}}{3}\cdot\left(\frac{0.5\cdot\mu m-\Delta L}{L-\Delta L}\right)^{n_P} + \frac{\left(\frac{L}{m}\right)^{n_P}}{a_P}\cdot V\right]$$ 3σ PMOS Threshold Variation

This equation from a process manufacturer shows two components of matching, which are a function of the length of a device and the spacing of the devices. The spacing term is insignificant for spacings below 0.3mm, so we will drop this term. The equation is also not a function of device width; it is fixed for 20mm transistors, so we will modify the equation to account for changing device widths below. The exponent is very close to 1/2, so we will use the square root instead.

$$\sigma_{\Delta VTP}(L) = \sigma_{VTPLmin}\cdot\sqrt{\left(\frac{L_{min}-\Delta L}{L-\Delta L}\right)\cdot\left(\frac{20\mu m-\Delta W}{W-\Delta W}\right)}$$ 3σ PMOS Threshold Variation

substituting in the constraint on W:

$$\sigma_{\Delta VTP}(L) = \sigma_{VTPLmin}\cdot\frac{V_{DSsat}}{L-\Delta L}\cdot\sqrt{(L_{min}-\Delta L)\cdot\mu\cdot C_{OX}\cdot\frac{20\mu m-\Delta W}{2\cdot I_{out}}}$$

Given a required specifcation on the threshold variance, we can find the required L.

$$L = \Delta L + \sigma_{VTPLmin}\cdot\frac{V_{DSsat}}{\sigma_{\Delta VTPdes}}\cdot\sqrt{(L_{min}-\Delta L)\cdot\mu_P\cdot C_{OX}\cdot\frac{20\mu m-\Delta W}{2\cdot I_{out}}}$$

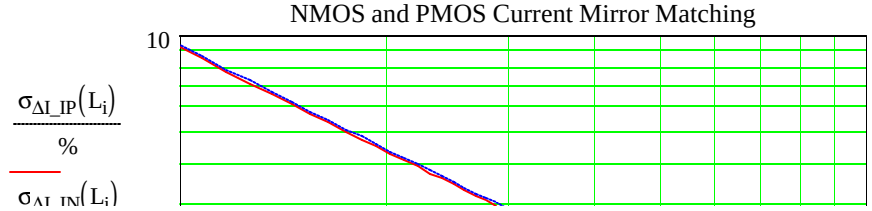
If we now substitute the V_T mismatch into the current mismatch equation

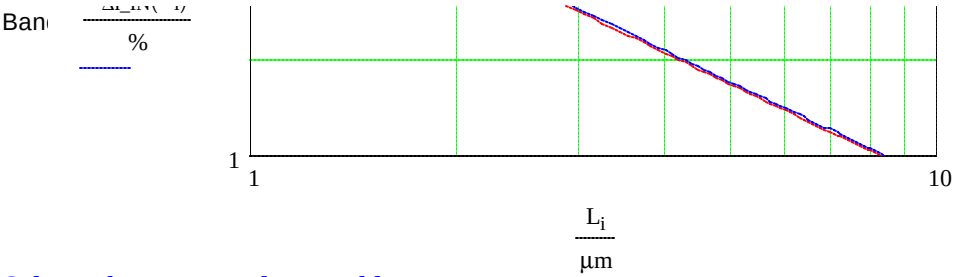
$$\sigma_{\Delta I\_IP}(L) := \sqrt{2^2\cdot\sigma_{\Delta VTPLmin}^2\cdot\frac{(L_{min}-\Delta L)}{(L-\Delta L)^2}\cdot\mu_P\cdot C_{OX}\cdot\frac{20\mu m-\Delta W}{2\cdot I_{out}} + \frac{\sigma_{\Delta W}^2}{M}\cdot\left[\frac{\mu_P\cdot C_{OX}\cdot V_{DSsat}^2}{2\cdot I_{out}\cdot(L-\Delta L)}\right]^2 + \frac{\sigma_{\Delta L}^2}{(L-\Delta L)^2}}$$

$$\sigma_{\Delta I\_IN}(L) := \sqrt{2^2\cdot\sigma_{\Delta VTNLmin}^2\cdot\frac{(L_{min}-\Delta L)}{(L-\Delta L)^2}\cdot\mu_N\cdot C_{OX}\cdot\frac{20\mu m-\Delta W}{2\cdot I_{out}} + \frac{\sigma_{\Delta W}^2}{M}\cdot\left[\frac{\mu_N\cdot C_{OX}\cdot V_{DSsat}^2}{2\cdot I_{out}\cdot(L-\Delta L)}\right]^2 + \frac{\sigma_{\Delta L}^2}{(L-\Delta L)^2}}$$

$$L_i := \frac{i}{num}\cdot 9.5\mu m + L_{min}$$ Length vector for plotting

NMOS and PMOS Current Mirror Matching





Solving this equation for L yields

$$L := \Delta L + \frac{1}{\sigma_{\Delta I\_Ides}} \cdot \sqrt{2^2 \cdot \sigma_{\Delta VTPLmin}^2 \cdot (L_{min} - \Delta L) \cdot \mu_P \cdot C_{OX} \cdot \frac{20\mu m - \Delta W}{2 \cdot I_{out}} + \frac{\sigma_{\Delta W}^2}{M} \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsat}^2}{2 \cdot I_{out}} \right)^2} + \sigma_{\Delta L}^2$$

$L = 4.17\,\mu m$

Normally, we think of larger V_{DSsat}s providing better current matching, but a larger V_{DSsat} requires a smaller width for a given current and length. The smaller width can hurt matching for small V_{DSsat}s. Also with smaller widths come smaller transistor area, which also hurts V_T matching. The net effect is DV_T's effect on current mismatch is not affected by changes in V_{DSsat}. Another perspective is to plot the area required vs. V_{DSsat} for a given current matching constraint.

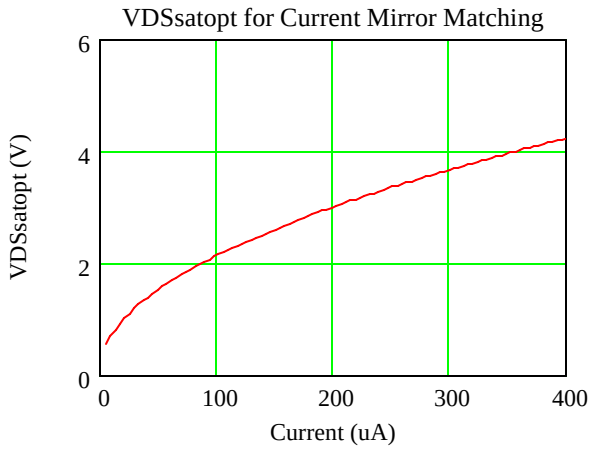
$$A := \frac{2^2 \cdot \left(\frac{\sigma_{\Delta VTPLmin}}{V_{DSsat}} \right)^2 \cdot (L_{min} - \Delta L) \cdot (20\mu m - \Delta W) + \frac{\sigma_{\Delta W}^2}{M} \cdot \frac{\mu_P \cdot C_{OX} \cdot V_{DSsat}^2}{2 \cdot I_{out}} + \frac{2 \cdot I_{out} \cdot \sigma_{\Delta L}^2}{\mu_P \cdot C_{OX} \cdot V_{DSsat}^2}}{\sigma_{\Delta I\_Ides}^2} \qquad \sqrt{A} = 46.5\,\mu m$$

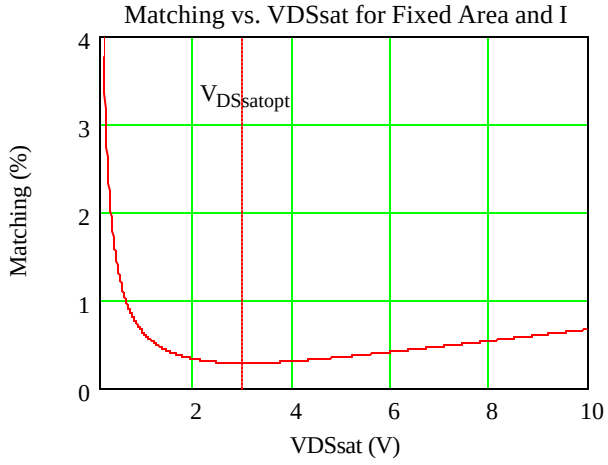
Here we see there is an optimal V_{DSsat} to minimize area for a given matching constraint:

$$V_{DSsatopt} := \sqrt[4]{\frac{\frac{4 \cdot I_{out} \cdot \sigma_{\Delta L}^2}{\mu_P \cdot C_{OX}} + 2^3 \cdot \sigma_{\Delta VTPLmin}^2 \cdot (L_{min} - \Delta L) \cdot (20\mu m - \Delta W)}{\frac{\sigma_{\Delta W}^2}{M} \cdot \frac{\mu_P \cdot C_{OX} \cdot 2}{2 \cdot I_{out}}}} \qquad V_{DSsatopt} = 3\,V$$

We can plot this a function of I

$$Ival_i := \frac{i}{num - 1} \cdot 2 \cdot I_{out}$$





We can also optimize current as to minimize area for a given matching constraint.

$$I_{opt} := \frac{1}{\sqrt{M}} \cdot \frac{\sigma_{\Delta W}}{\sigma_{\Delta L}} \cdot \frac{\mu_P \cdot C_{OX}}{2} \cdot V_{DSsat}^2 \qquad I_{opt} = 2.03\,\mu A$$

We can also combine the optimal matching current and V_{DSsat} equations to find the optimal current source

matching to minimize area for a given matching constraint.

$$V_{DSsatopt} := \sqrt{\frac{4}{3}}\cdot\sqrt{M}\cdot\sigma_{\Delta VTPLmin}\cdot\sqrt{\frac{L_{min}-\Delta L}{\sigma_{\Delta L}}\cdot\frac{20\mu m-\Delta W}{\sigma_{\Delta W}}} \qquad V_{DSsatopt} = 0.37\,V$$

$$I_{opt} := \sqrt{M}\cdot\mu_P\cdot C_{OX}\cdot\frac{2}{3}\cdot\frac{L_{min}-\Delta L}{\sigma_{\Delta L}}\cdot\frac{20\mu m-\Delta W}{\sigma_{\Delta L}}\cdot\sigma_{\Delta VTPLmin}^{2} \qquad I_{opt} = 3.05\,\mu A$$

What we find is that most of these equations are not interesting for most applications, except maybe watch makers. For typical currents required by noise and settling time constraints, the optimal V_{DSsat}'s are larger than the ones optimal for dynamic range.

Improved matching required increased area, which reduces the bandwidth of the circuit it is attached. Below is an equation for the bandwidth of a current mirror of the a device given length.

$$\omega_T = \frac{g_m}{C_{gs}+M\cdot C_{gs}} = \frac{\mu\cdot V_{DSsat}}{(L-\Delta L)^2\cdot(M+1)}$$

This can be solved for L and substitute into the current mismatch equation

$$L-\Delta L = \sqrt{\frac{\mu\cdot V_{DSsat}}{\omega_T\cdot(M+1)}}$$

$$\omega_T := \frac{\sigma_{\Delta I\_Ides}^{2}}{M+1}\cdot\frac{1}{\left[2^2\cdot\sigma_{\Delta VTPLmin}^{2}\cdot(L_{min}-\Delta L)\cdot\frac{C_{OX}}{V_{DSsat}}\cdot\frac{20\mu m-\Delta W}{2\cdot I_{out}}+\frac{\sigma_{\Delta W}^{2}}{M\cdot\mu_P\cdot V_{DSsat}}\cdot\left(\frac{\mu_P\cdot C_{OX}\cdot V_{DSsat}^{2}}{2\cdot I_{out}}\right)^2+\frac{\sigma_{\Delta L}^{2}}{\mu_P\cdot V_{DSsat}}\right]} \qquad \frac{\omega_T}{2\cdot\pi} = 8.24\,MHz$$

Thus we can see a fast degradation of w_T as mismatch requirements increase. V_{DSsat} can also be optimized to maximize w_T, given matching and current requirements

$$V_{DSsat} := \sqrt[4]{\frac{M+1}{3}\cdot\left[\frac{(2\cdot I_{out})^2\cdot\sigma_{\Delta L}^{2}}{C_{OX}^{2}\cdot\mu_P^{2}\cdot\sigma_{\Delta W}^{2}}+2^2\cdot\sigma_{\Delta VTPLmin}^{2}\cdot 2\cdot I_{out}\cdot(L_{min}-\Delta L)\cdot\frac{20\mu m-\Delta W}{\mu_P\cdot C_{OX}\cdot\sigma_{\Delta W}^{2}}\right]} \qquad V_{DSsat} = 2.53\,V$$

One of the best ways to use these design equations to choose a current, I, and length, L, to provide the desired matching and bandwidth. It is difficult to come up with a neat closed form expression for I, but rather it is done here in the form of a quadratic

$$\left[\sigma_{\Delta I\_Ides}^{2}-\frac{\sigma_{\Delta L}^{2}}{\frac{\mu\cdot V_{DSsat}}{\omega_T\cdot(M+1)}}\right]\cdot I_{out}^{2} = 2^2\cdot\sigma_{\Delta VTPLmin}^{2}\cdot\frac{(L_{min}-\Delta L)}{\frac{\mu\cdot V_{DSsat}}{\omega_T\cdot(M+1)}}\cdot\mu\cdot C_{OX}\cdot\frac{20\mu m-\Delta W}{2}\cdot I_{out}+\frac{\sigma_{\Delta W}^{2}}{M\cdot\frac{\mu\cdot V_{DSsat}}{\omega_T\cdot(M+1)}}\cdot\left(\frac{\mu\cdot C_{OX}\cdot V_{DSsat}^{2}}{2}\right.$$

$$a := \sigma_{\Delta I\_Ides}^{2}-\frac{\sigma_{\Delta L}^{2}}{\frac{\mu_P\cdot V_{DSsat}}{\omega_T\cdot(M+1)}} \qquad b := -\left[2\cdot\sigma_{\Delta VTPLmin}^{2}\cdot\frac{(L_{min}-\Delta L)}{\frac{\mu_P\cdot V_{DSsat}}{\omega_T\cdot(M+1)}}\cdot\mu_P\cdot C_{OX}\cdot(20\mu m-\Delta W)\right]$$

$$c := \frac{-\sigma_{\Delta W}^{2}}{M\cdot\frac{\mu_P\cdot V_{DSsat}}{\omega_T\cdot(M+1)}}\cdot\left(\frac{\mu_P\cdot C_{OX}\cdot V_{DSsat}^{2}}{2}\right)$$

$$I_{req} := \frac{b}{2\cdot a}\cdot\left(1-\sqrt{1-\frac{4\cdot c}{b^2}}\right) \qquad I_{req} = 2.75\times 10^{3}\,\mu A \qquad \frac{\omega_T}{2\cdot\pi} = 8.24\,MHz$$

Current Mirror Variance

Bandgap Voltage Variance Derivation

Random Component Variations

$$I_4 = I \qquad I_5 = I + \Delta I \qquad I_{S5} = I_S \qquad I_{S4} = N \cdot I_S \cdot \left(1 + \frac{\Delta I_S}{\sqrt{N}}\right)$$

$$R_1 = R \qquad R_2 = \frac{K_{ptat}}{2 \cdot \ln(N)} \cdot R \cdot \left(1 + \frac{\Delta R}{R \cdot \sqrt{\frac{K_{ptat}}{2 \cdot \ln(N)}}}\right)$$

PTAT Current Generator Variance:, Sum of the voltages around a loop

$$V_{BE4} + R_1 \cdot I_4 = V_{BE5}$$

$$I_4 = \frac{V_{BE5} - V_{BE4}}{R_1} = \frac{V_T \cdot \ln\left(\frac{I_4}{I_{S4}}\right) + V_T \cdot \ln\left(\frac{I_5}{N \cdot I_{S5}}\right)}{R_1} = \frac{V_T \cdot \ln\left[\frac{I \cdot \left(1 - \frac{\Delta I}{2 \cdot I}\right)}{I_S}\right] + V_T \cdot \ln\left[\frac{I \cdot \left(1 + \frac{\Delta I}{2 \cdot I}\right)}{N \cdot I_S \cdot \left(1 - \frac{\sigma_{\Delta IS\_IS}}{\sqrt{N}}\right)}\right]}{R_1}$$

$$I_4 = \frac{V_T \cdot \sqrt{\sigma_{\Delta I\_I}^2 + \frac{\sigma_{\Delta IS\_IS}^2}{N}} + V_T \cdot \ln(N)}{R_1} \qquad I = \frac{V_T \cdot \left(-\sigma_{\Delta I\_I} + \frac{\sigma_{\Delta IS\_IS}}{N}\right) + V_T \cdot \ln(N)}{R_1}$$

The variance for the output voltage is given as follows

$$V_{bg} = V_{BE5} + (I_4 + I_5) \cdot R_2$$

Substitute in the variables and simplify:

$$\sigma_{\Delta Vbg\_Vbg}^2 = V_T^2 \cdot \left[\left(1 + \frac{1}{\ln(N)} + \frac{I \cdot R_2}{V_T}\right)^2 \cdot \sigma_{\Delta I\_Imir}^2 + \sigma_{\Delta Is\_Is}^2 \cdot \left(\frac{K_{ptat}}{\ln(N) \cdot \sqrt{N}}\right)^2 + \sigma_{\Delta R\_R}^2 \cdot K_{ptat} \cdot 2 \cdot \ln(N)\right]$$

The variance in K is given as

$$\sigma_{\Delta K\_K} = \frac{1}{\ln(N)} \cdot \sqrt{\sigma_{\Delta I\_I}^2 + \frac{\sigma_{\Delta IS\_IS}^2}{N} + \ln(N)^2 \cdot \sigma_{\Delta R\_R}^2}$$

For design we substitute the following variables:

$$\sigma_{\Delta R\_R}^2 = \frac{\sigma_{\Delta R\_R.min}^2 \cdot W_{min}^2}{W_R^2} \quad \text{where} \qquad \sigma_{\Delta R\_R.min} := \sqrt{\frac{\left(\frac{R_{sq} \cdot \sigma_{\Delta L}}{R_1}\right)^2 + \sigma_{\Delta W}^2}{W_{min}^2}} \qquad \sigma_{\Delta R\_R.min} = 0.26$$

$$\sigma_{\Delta VTP}^2 = \Delta V_{thPLmin}^2 \cdot \frac{L_{min}^2}{L_P^2} \quad \text{3s PMOS Threshold Variation, where}$$

$$\Delta V_{thPLmin} := \sqrt{\sigma_{\Delta VTPLmin}^2 \cdot V_{DSsat}^2 \cdot \mu_P \cdot C_{OX} \cdot \frac{20\mu m}{2 \cdot I \cdot L_{min}}} \qquad \Delta V_{thPLmin} = 68.3\,mV$$

$$\sigma_{\Delta VTN}^2 = \Delta V_{thLnmin}^2 \cdot \frac{L_{min}^2}{L_N^2} \quad \text{3s NMOS Threshold Variation, where}$$

$$\Delta V_{thNLmin} := \sqrt{\sigma_{\Delta VTNLmin}^2 \cdot V_{DSsat}^2 \cdot \mu_N \cdot C_{OX} \cdot \frac{20\mu m}{2 \cdot I \cdot L_n}} \qquad \Delta V_{thNLmin} = 97.3\,mV$$

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$$\sigma_{\Delta I\_Imir}^2 = \Delta V_{thPLmin}^2 \cdot \frac{L_{min}^2}{L_P^2} \cdot \left(\frac{2}{V_{DSsatP}} \right)^2 + \sigma_{\Delta W}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}{2 \cdot I \cdot L_P} \right)^2 + \frac{\sigma_{\Delta L}^2}{L_P^2}$$ Current Mirror Mismatch

$$\sigma_{\Delta Is\_Is}^2 = \sigma_{\Delta Is\_IsAreamin}^2 \cdot \frac{Area_{BJTmin}}{Area_{Q1}}$$ Bipolar Transistor Reverse Saturation Current Mismatch

Thus the mismatch equation becomes

$$\sigma_{\Delta Vbg\_Vbg}^2 = \frac{V_T^2}{V_{bg}^2} \cdot \left[\left(1 + \frac{1}{\ln(N)} + \frac{I \cdot R_2}{V_T} \right)^2 \cdot \left[\Delta V_{thPLmin}^2 \cdot \frac{L_{min}^2}{L_P^2} \cdot \left(\frac{2}{V_{DSsatP}} \right)^2 + \sigma_{\Delta W}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}{2 \cdot I \cdot L_P} \right)^2 + \frac{\sigma_{\Delta L}^2}{L_P^2} \right] + \frac{\sigma_{\Delta Is}}{}$$

The mismatch can be expressed in the following simplified form, which is useful for optimization:

$$\sigma_{\Delta Vbg\_Vbg}^2 = \frac{X_1}{L_P^2} + \frac{X_2}{Area_{Q1}} + \frac{X_3}{W_R^2}$$

where the coefficients are

$$X_1 := \left(\frac{V_T}{V_{bg}} \right)^2 \cdot \left(1 + \frac{1}{\ln(N)} + \frac{I \cdot R_2}{V_T} \right)^2 \cdot \left[\Delta V_{thPLmin}^2 \cdot L_{min}^2 \cdot \left(\frac{2}{V_{DSsatP}} \right)^2 + \sigma_{\Delta W}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}{2 \cdot I} \right)^2 + \sigma_{\Delta} \right]$$

$$\sqrt{X_1} = 2.95\,\%\cdot\mu m$$

$$X_2 := \left(\frac{V_T}{V_{bg}} \right)^2 \cdot \frac{\sigma_{\Delta Is\_IsAreamin}^2 \cdot Area_{BJTmin} \cdot K_{ptat}^2}{\ln(N)^2 \cdot N}$$

$$\sqrt{X_2} = 1.63\,\%\cdot\mu m$$

$$X_3 := \left(\frac{V_T}{V_{bg}} \right)^2 \cdot \sigma_{\Delta R\_R.min}^2 \cdot W_{min}^2 \cdot K_{ptat} \cdot 2 \cdot \ln(N)$$

$$\sqrt{X_3} = 5\,\%\cdot\mu m$$

The main goal is to minimize total cost, which effectively achieved by minimized total area. Minimizing totla area requires optimization routines. Minimizing total active area is a good approximation

$$Area = 2 \cdot \frac{2 \cdot I \cdot L_P}{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2} \cdot L_P + (N + 1) \cdot Area_{Q1} + \frac{W_R^2}{R_{sq}} \cdot (R_1 + R_2)$$

The active area can be expressed in the following form, which is useful for optimization:

$$Area = Y_1 \cdot L_P^2 + Y_2 \cdot Area_{Q1} + Y_3 \cdot W_R^2$$

where the coefficients are

$$Y_1 := \frac{2 \cdot I}{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}$$

$$\sqrt{Y_1} = 2.67 \frac{\mu m}{\mu m}$$ Area Coefficient for PMOS Length

$$Y_2 := N + 1$$

$$\sqrt{Y_2} = 3 \frac{\mu m}{\mu m}$$ Area Coefficient for BJT Area

$$Y_3 := \frac{R_1 + R_2}{R_{sq}}$$

$$\sqrt{Y_3} = 1.5 \frac{\mu m}{\mu m}$$ Area Coefficient for Resistor Width

From these variables we can find the minimum total active area using a previous derivation.

$$Area_{opt} := \frac{\left(\sqrt{Y_1 \cdot X_1} + \sqrt{Y_2 \cdot X_2} + \sqrt{Y_3 \cdot X_3} \right)^2}{\sigma_{\Delta Vbg\_Vbg}^2}$$

$$\sqrt{Area_{opt}} = 6.75\,\mu m$$ Minimum Total Area

The minimum total area is used to find the required resistor widths and MOSFET lengths for matching.

$$L_P := \sqrt{\sqrt{\frac{Area_{opt}}{\sigma_{\Delta Vbg\_Vbg}^2} \cdot \frac{X_2}{Y_2}}}$$

$$L_P = 1.11\,\mu m$$ Optimal PMOS Device Length

$$Area_{Q1} := \sqrt{\frac{Area_{opt}}{\sigma_{\Delta Vbg\_Vbg}^2} \cdot \frac{X_3}{Y_3}}$$

$$\sqrt{Area_{Q1}} = 2.74\,\mu m$$ Optimal BJT Area

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$$W_R := \sqrt{\frac{Area_{opt}}{\sigma_{\Delta Vbg\_Vbg}^2} \cdot \frac{X_1}{Y_1}} \qquad W_R = 1.58\,\mu m$$ Optimal Resistor Width

When sizing the length we have to meet both the 1/f noise constraint and the matching constraint, so here we pick the larger of the two. To minimize area when the length constraint is longer for 1/f noise, we should recalculate the required resistor and BJT areas for matching.With the exact length sizing known, we have place constraints based on the minimum length, and incremental values. These length constraints are calculated in the following function.

$$L_P := L_{fix}\left[if\left[No1\_f, L_P, \max\left(\left(L_P \quad L_{P1\_f} \right) \right) \right] \right] \qquad L_P = 2\,\mu m$$

$$W_R := W_{fix}(W_R) \qquad W_R = 1.6\,\mu m$$

$$Area_{Q1} := Area_{fix}(Area_{Q1}) \qquad \sqrt{Area_{Q1}} = 4.47\,\mu m$$

Other Sizing Calculations

With the PMOS length calculated, we can find the required PMOS lengths based on VDSsat and curret requirements:

$$W_P := \frac{2 \cdot I \cdot L_P}{\mu_P \cdot C_{OX} \cdot \left(1 - \sigma_{\mu PCOX}\right) \cdot V_{DSsat}^2} \qquad W_P = 1.7\,\mu m$$ PMOS Transistor Width

If the width is shorter than the minimum width we constrain it and resize the length.

$$W_P := W_{fix}(W_P) \qquad W_P = 1.7\,\mu m$$

$$L_P := \frac{\mu_P \cdot C_{OX} \cdot W_P}{2 \cdot I} \cdot \left(1 - \sigma_{\mu PCOX}\right) \cdot V_{DSsat}^2 \qquad L_P = 2\,\mu m$$

The resistor lengths are found from the calculated from the widths and the resistor values.

$$W_R := if\left(\frac{W_R \cdot R_1}{R_{sq}} < L_{min}, \frac{L_{min} \cdot R_{sq}}{R_1}, W_R \right) \qquad W_R = 1.6\,\mu m$$

$$L_{R1} := \frac{W_R \cdot R_1}{R_{sq}} \qquad L_{R1} = 0.61\,\mu m$$ Length of Resistor R_1

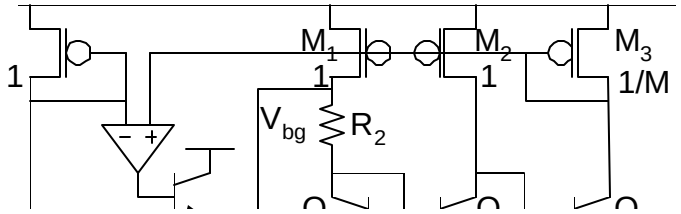
$$L_{R2} := \frac{W_R \cdot R_2}{R_{sq}} \qquad L_{R2} = 2.98\,\mu m$$ Length of Resistor R_2

Bandgap Variance Derivation

Start-Up Circuitry

Start-Up Circuitry

Most self-bias circuits, such as bandgaps have two stable operating points. One of the stable operating states is the desired state and the other is typically a zero-current state. To prevent the zero-current state from occuring a start-up circuit is added, which is active during the undesired state and inactive during the desired state. The following figures illustrate several start-up circuits for the bandgap above. Simple modifications to these start-ups can be made for other bandgap topologies.



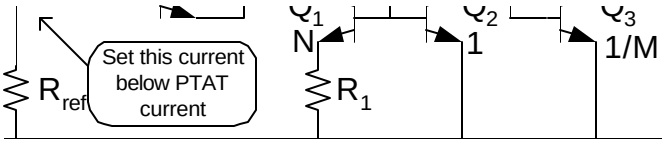


Fig. 1: Bandgap with Op-Amp Based Start-Up Circuit

The op-amp based start-up circuit has a simple design procedure:

1. Pick a bias voltage in the bandgap.
2. Find the two stable operating points for the bias voltage.
3. Set a compare voltage between the two stable operating voltages.
4. Amplifiy the difference and apply it to the gate of a transistor., so the transistor turns off for the desired operating point and turns on for the undesired. The transistor is used to inject current into the circuit in the undesired state. Here is another version of the circuit above:

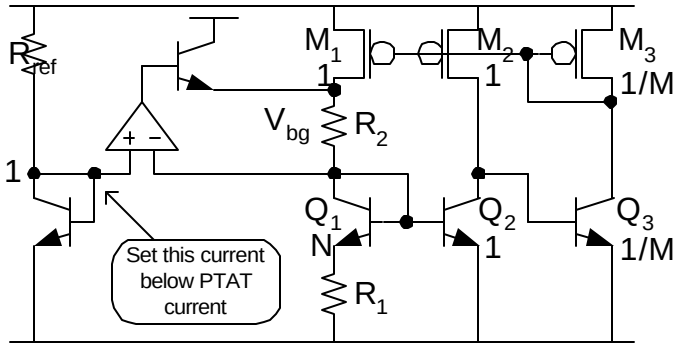


Fig. 1: Sensitive Op-Amp Based Start-Up Circuit

Here the start-up circuit comparison voltage is from a node, which varies less than the in the previous circuit. With less variation in the comparison voltage, the circuit is more likely to switch to the wrong operating point with process variations and offsets in the amplifier. It is best to choose a node in the circuit with the largest variation between the two operating points. In bandgaps, this node is usually the bandgap voltage itself. The bandgap voltage difference between the two operating points is so large that the op-amp can be eliminated as in the following start-up circuit.

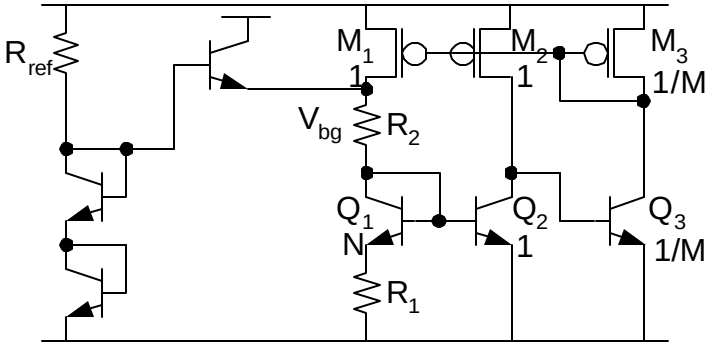
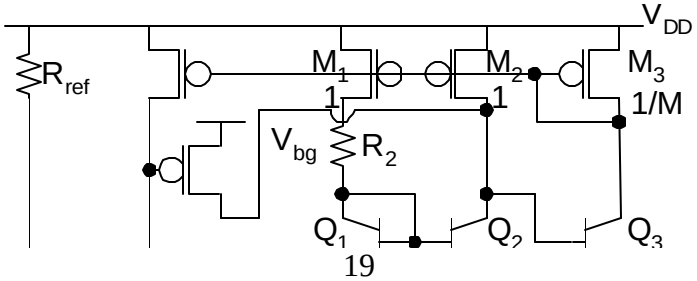


Fig. 1: Source Follower Based Start-Up Circuit

It is also possible to combine the reference voltage and the operational amplifier, or to use a compare current as in the following circuit.



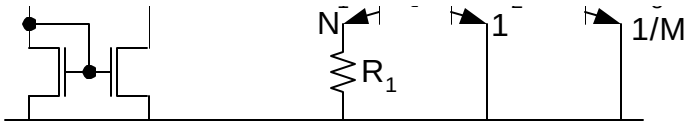


Fig. 1: Current mirror based start-up circuit.

In all of the start-up examples above, the start-up circuit consumes static current. This current can be made small and thus unimportant relative to the current of the bandgap itself. It is possible to make the start-up consume zero current by making it bi-stable as well. If the bandgap is in it's desired state the start-up is forced into a zero current state. If the bandgap is in the undesired state, the startup circuit's current is active until the bandgap goes back to the desired state. This method for eliminating the current in the bandgap involves more risk, because the comparison point may shift when the start-up current is off.

When a start-up circuit is used with a PTAT current generator, the internal voltage swings are usually too small to use without amplification. For PTAT current generators it is best to use a current mirror type of start-up circuit.

Start-Up Circuitry

BiCMOS Bandgap Performance

Area of Circuit

$Area_{BJT} := (N + 1)\cdot Area_{Q1}$ $\sqrt{Area_{BJT}} = 13.42\,\mu m$ BJT Area

$Area_R := W_R\cdot(L_{R1} + L_{R2})$ $\sqrt{Area_R} = 2.4\,\mu m$ Resistor Area

$Area_{CAP} := 0\mu m^2$ $\sqrt{Area_{CAP}} = 0\,\mu m$ Capacitor Area

$Area_{MOS} := 2\cdot W_P\cdot(L + 2\cdot 3\cdot L_{min})$ $\sqrt{Area_{MOS}} = 4.94\,\mu m$ MOS Area

$Area := (Area_R + Area_{CAP} + Area_{BJT} + Area_{MOS})$ $\sqrt{Area} = 14.5\,\mu m$ Total Area

Power Dissipation of Circuit

$I_{VDD} := 2\cdot I$ $I_{VDD} = 147.22\,\mu A$ Current from Supply

$Power := 2\cdot I\cdot V_{DD}$ $Power = 0.44\,mW$ Power Dissipation

Cost of Circuit (Including Power)

$C_A := 5\frac{cents}{mm^2}$ $C_P := \frac{40cents}{2.7V\cdot 200mA}$

$Cost := C_A\cdot Area + C_P\cdot Power$ $Cost = 0.03\,cents$

Plots

$$\sigma_{\Delta Vo\_Vo}(T) := V_T\cdot\frac{T}{Temp}\cdot\sqrt{\left(1 + \frac{1}{\ln(N)} + \frac{I\cdot R_2}{V_T\cdot\frac{T}{Temp}}\right)^2\cdot\left[\Delta V_{thPLmin}^2\cdot\frac{L_{min}^2}{L_P^2}\cdot\left(\frac{2}{V_{DSsatP}}\right)^2 + \sigma_{\Delta W}^2\cdot\left(\frac{\mu_P\cdot C_{OX}\cdot V_{DSsatP}^2}{2\cdot I\cdot L_P}\right)^2 + \frac{\sigma_{\Delta}}{L}\right.}$$

$\frac{\sigma_{\Delta Vo\_Vo}(Temp)}{V_{bg}} = 3.48\,\%$

$\sigma_{\Delta Vbg} := \sigma_{\Delta Vo\_Vo}(Temp)$ $\sigma_{\Delta Vbg} = 44.53\,mV$

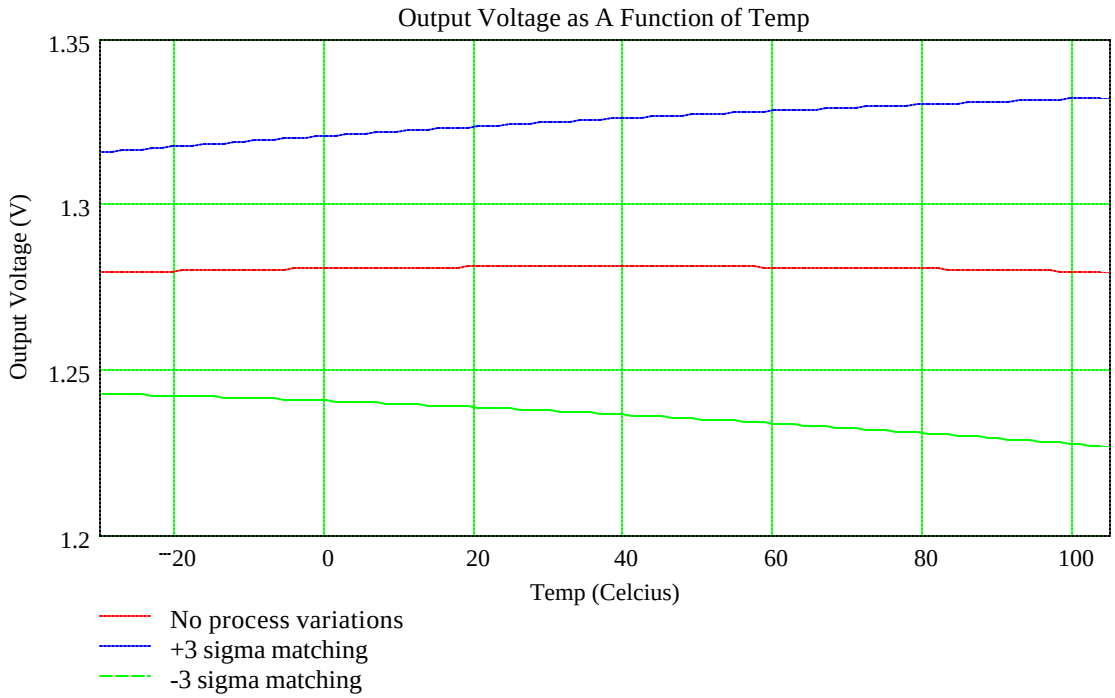
$V_{osig3p}(T) := V_{G0} + \frac{k\cdot T}{q}\cdot(\gamma - \alpha)\cdot\left(1 + \ln\left(\frac{Temp}{T}\right)\right) + \sigma_{\Delta Vo\_Vo}(T)$

$V_{bgmax} := V_{osig3p}(Temp)$ $V_{bgmax} = 1.33\,V$ Maximum Bandgap Voltage

Ban

$$V_{osig3n}(T) := V_{G0} + \frac{k \cdot T}{q} \cdot (\gamma - \alpha) \cdot \left(1 + \ln\left(\frac{Temp}{T}\right)\right) - \sigma_{\Delta Vo\_Vo}(T)$$

$V_{bgmin} := V_{osig3n}(Temp)$ $\quad V_{bgmin} = 1.24\,V$ Minimum Bandgap Voltage



One interesting point can be seen from the plot of the bandgap voltage with process variations is that the bandgap voltage varies more with process variations than it does with temperature. Care must be taken, when designing curvature correction circuits for bandgaps, to make sure the variations are not limited by random variations.

$$g_m := \frac{I}{V_T} \qquad g_{mP} := \frac{2 \cdot I}{V_{DSsatP}}$$

$$v_{nQ1} := \sqrt{4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot g_m}} \qquad v_{nQ1} = 1.77\,\frac{nV}{\sqrt{Hz}}$$

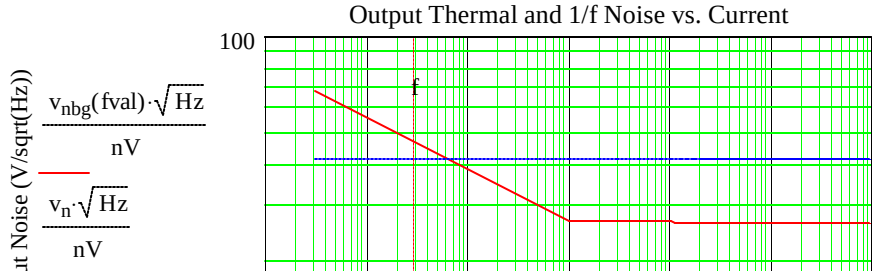
$$v_{nQ2} := \sqrt{4 \cdot k \cdot Temp \cdot \frac{1}{2 \cdot g_m}} \qquad v_{nQ2} = 1.77\,\frac{nV}{\sqrt{Hz}}$$

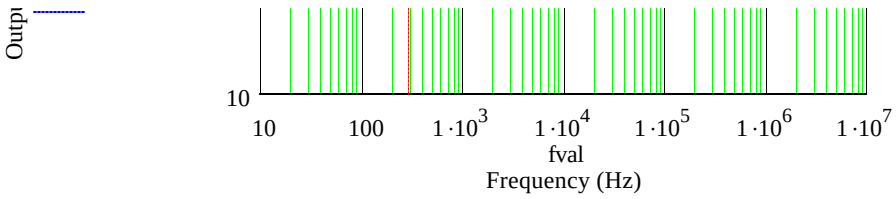
$$v_{nR1} := \sqrt{4 \cdot k \cdot Temp \cdot R_1} \qquad v_{nR1} = 3.61\,\frac{nV}{\sqrt{Hz}}$$

$$v_{nR2} := \sqrt{4 \cdot k \cdot Temp \cdot R_2} \qquad v_{nR2} = 8\,\frac{nV}{\sqrt{Hz}}$$

$$v_{nM1}(f) := \sqrt{4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot g_{mP}} + \frac{K_{fP}}{W_P \cdot L_P \cdot f}} \qquad v_{nM1}(f) = 32.25\,\frac{nV}{\sqrt{Hz}}$$

$$v_{nbg}(f) := \sqrt{\frac{\left(R_2 \cdot g_m + 1\right)^2 \cdot {v_{nR1}}^2 + \left(1 + R_2 \cdot g_m + \ln(N)\right)^2 \cdot {v_{nQ2}}^2 + \left(R_2 \cdot g_m + 1\right)^2 \cdot {v_{nQ1}}^2 + \left(\frac{g_{mP}}{g_m}\right)^2 \cdot \left(1 + R_2 \cdot g_m + \ln(N)\right)^2 \cdot 2 \cdot v_{nM}}{\ln(N)^2}}$$





$W_P := W_P$
$L_P := L_P$
$N := N$
$R_1 := R_1$
$R_2 := R_2$
$Area_{Q1} := Area$

BiCMOS Bandgap Performance

$Cost = 0.03\,cents$

$V_{DDbgmin} = 2.12\,V$

$\sqrt{Area} = 14.5\,\mu m$

$Power = 0.44\,mW$

$I_{VDD} = 147.22\,\mu A$

$v_n = 41.44\,\frac{nV}{\sqrt{Hz}}$

$\sigma_{\Delta Vbg\_Vbg} = 3\,\%$

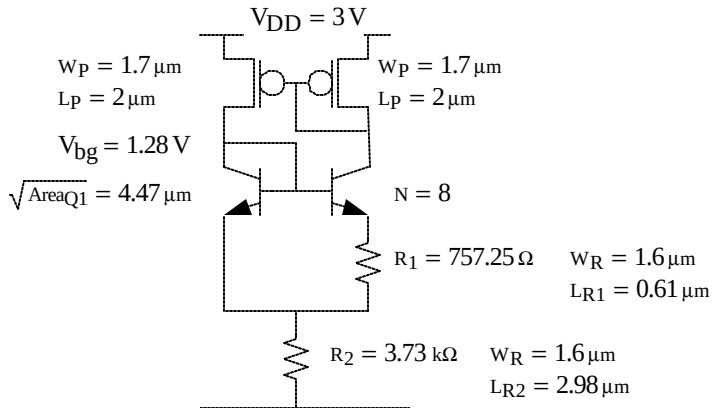


Fig. 1: Basic BiCMOS bandgap with device sizes and performance

OpAmp VtoI w/ NMOS Follower

Option #1: Mirror Bandgap Current from Bandgap's Emitter Follower:

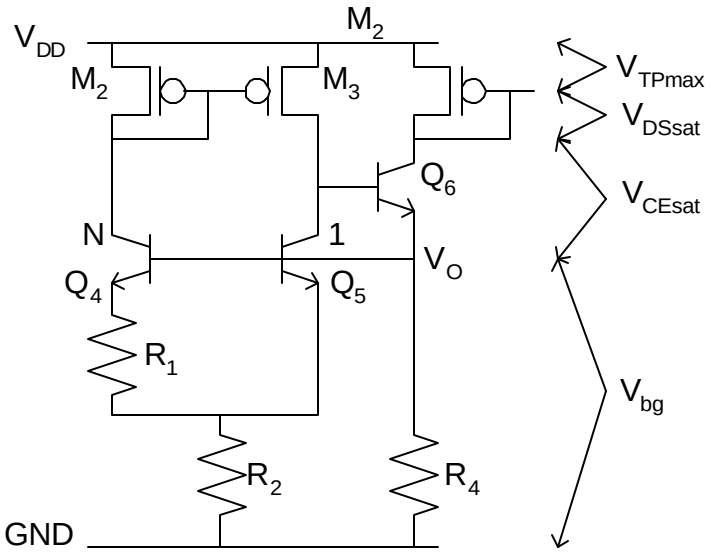


Fig. 1: Bandgap Current Generator Circuit (Option #1)

There are several ways to generate a bandgap current. The easiest method is mirror off the bandgap current directly from collector of the emitter follower, Q_6, in the bandgap circuit. This method doesn't work for supply voltages below ($V_{bg} + V_{CEsat} + V_{TPmax} + V_{DSsatmin}$)=2.63V. Current technology requires a minimum supply voltage of 2.7V, which will be changing to 2.25V in the near future. To be safe, it is best to use another bandgap circuit, which will work with low power supplies.

$V_{DDminoption1} := V_{bgmax} + V_{CEsat} + V_{TPmax} + V_{DSsatmin}$ $V_{DDminoption1} = 2.73\,V$

If larger supplies are available, it is usually best to maximize V_{DSsat}s to reduce noise. In this case for design an upper limit is set on V_{DSsat}:

$V_{DSsatmax} := V_{DDmin} - (V_{bgmax} + V_{CEsat} + V_{TPmax})$ $\quad V_{DSsatmax} = 0.17\,V$

Variance in Output Current

Other than headroom a minor downfall of this option is the variance in the output current due to base current variation from the bandgap transistors.

$$I_o = \left(\frac{V_{bg}}{R_{ext}} + 2\cdot I_b\right)\cdot M = \left(\frac{V_{bg}}{R_{ext}} + \frac{2\cdot I}{\beta}\right)\cdot M = \left[\frac{V_{bg}\cdot(1+\sigma_{\Delta Vbg\_Vbg})}{R_{ext}\cdot(1+\sigma_{\Delta Rext\_Rext})} + \frac{2\cdot I\cdot(1+\sigma_{\Delta I\_I})}{\beta\cdot(1+\sigma_{\Delta\beta\_\beta})}\right]\cdot M$$

The variance in the output current is calculated with the following substitutions:

$$I = I\cdot(1+\sigma_{\Delta I\_I}) \quad \beta = \beta\cdot(1+\sigma_{\Delta\beta\_\beta}) \quad R_{ext} = R_{ext}\cdot(1+\sigma_{\Delta Rext\_Rext}) \quad V_{bg} = V_{bg}\cdot(1+\sigma_{\Delta Vbg\_Vbg})$$

To yield the following equation:

$$I_o + \sigma_{\Delta Io} = \frac{V_{bg}\cdot(1+\sigma_{\Delta Vbg\_Vbg})}{R_{ext}\cdot(1+\sigma_{\Delta Rext\_Rext})} + \frac{2\cdot I\cdot(1+\sigma_{\Delta I\_I})}{\beta\cdot(1+\sigma_{\Delta\beta\_\beta})}$$

This can be simplified to find the variance in the output current:

$$\sigma_{\Delta Io\_Io} = \frac{I_o - 2\cdot I_b}{I_o}\cdot(\sigma_{\Delta Vbg\_Vbg} + \sigma_{\Delta Rext\_Rext}) + 2\cdot\frac{I_b}{I_o}\cdot(\sigma_{\Delta I\_I} + \sigma_{\Delta\beta\_\beta})$$

From this equation we can get insight into the sizing of I_o (and thus R_{ext}) to suppress variances in Beta.

Current Noise Calculations

It might be best to quantify the output noise in terms of a noise voltage so that options 1, 2 and 3 can be compared accurately. The noise voltage would be defined at noise at the output of the gate of the PMOS current mirror. Note that these noise derivation will put constraints on R_{ext} and g_{mi} in the op-amp section.The noise in the output current is:

$$\sigma_{Ion}^2 = \left[\left(\frac{V_{bgn}}{R_{ext}}\right)^2 + 2\cdot 2\cdot q\cdot I_b + 4\cdot k\cdot Temp\cdot\frac{1}{R_{ext}}\right]\cdot M^2 + 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}} + 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}}\cdot M$$

We can use the following expression for the output current to solve for M.

$$I_o = M\cdot\frac{V_{bg}}{R_{ext}} \qquad M = \frac{I_o\cdot R_{ext}}{V_{bg}}$$

At the same time we substitute in the expression for the base current I_b.

$$I_b = \frac{V_{bg}}{\beta\cdot R_{ext}}$$

M is substituted into the bandgap expression to solve for R_{ext}.

$$\sigma_{Ion}^2 = \left[\left(\frac{V_{bgn}}{R_{ext}}\right)^2 + 2\cdot 2\cdot q\cdot\frac{V_{bg}}{\beta\cdot R_{ext}} + 4\cdot k\cdot Temp\cdot\frac{1}{R_{ext}}\right]\cdot\left(\frac{I_o\cdot R_{ext}}{V_{bg}}\right)^2 + 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}} + 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}}\cdot\frac{I_o\cdot R_{ext}}{V_{bg}}$$

The noise from the last mirror transistor is subtracted off and the expression is simplified

$$\sigma_{Ion}^2 - 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}} = \frac{V_{bgn}^2}{V_{bg}^2}\cdot I_o^2 + \left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)\cdot 4\cdot k\cdot Temp\cdot I_o^2\cdot\frac{R_{ext}}{V_{bg}}$$

We substitute in a quick approximation for the noise of the bandgap to help us budget the noise.

$\sigma_{Vbgn}^2 = 4\cdot k\cdot Temp\cdot K_{ptat}^2\cdot\frac{V_T}{I}$ bandgap quick approximation (K_{ptat} is on the order of 20)

Now we see several noise terms. The basic bandgap noise, base current noise, resistor noise, and current mirror noise

Now we see several noise terms: The basic bandgap noise, base current noise, resistor noise, and current mirror noise. Thus for the same current the bandgap contributes 65%(V_{DSsat}=200mV)-80%(V_{DSsat}=1V) and the resistor about 10%, the base current about 5%, and the current mirror about 35%. The budgeting is a significant function of V_{DSsat}, but we'll assume 75% for the bandgap and 25% for the other components, which are fixed by the resistor value.

$$\sigma_{Ion}^2 - 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}} = 4\cdot k\cdot Temp\cdot I_o^2\cdot\left[\frac{K_{ptat}^2\cdot V_T\cdot 2}{V_{bg}^2\cdot I} + \left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)\cdot\frac{1}{I}\right]$$

$$\frac{\frac{K_{ptat}^2\cdot V_T\cdot 2}{V_{bg}^2}}{\left[\frac{K_{ptat}^2\cdot V_T\cdot 2}{V_{bg}^2} + \left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)\right]} = 89.06\%$$ Bandgap

$$\frac{\frac{1}{V_{bg}}}{\left[\frac{K_{ptat}^2\cdot V_T\cdot 2}{V_{bg}^2} + \left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)\right]} = 5.08\%$$ Resistor

$$\frac{\frac{1}{V_T}\cdot\frac{1}{\beta}}{\frac{K_{ptat}^2\cdot V_T\cdot 2}{V_{bg}^2} + \left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)} = 2.43\%$$ Base Current

$$\frac{\frac{1}{3\cdot V_{DSsat}}}{\frac{K_{ptat}^2\cdot V_T\cdot 2}{V_{bg}^2} + \left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)} = 3.43\%$$ Current Mirror

Now we can size the current-setting resistor

$$R_{ext} := \frac{\left(\sigma_{Ion}^2 - 4\cdot k\cdot Temp\cdot\frac{2\cdot 2\cdot I_o}{3\cdot V_{DSsat}}\right)\cdot 25\%}{\left(\frac{1}{V_T}\cdot\frac{1}{\beta} + \frac{1}{V_{bg}} + \frac{2\cdot 2}{3\cdot V_{DSsat}}\right)\cdot\frac{4\cdot k\cdot Temp\cdot I_o^2}{V_{bg}}} \qquad R_{ext} = 311.23\,k\Omega$$

Now the value for M can be found

$$M := \frac{I_o\cdot R_{ext}}{V_{bg}} \qquad M = 3.89$$ Current Mirror Ratio

OpAmp VtoI w/ NMOS Follower

CMOS Bandgap

CMOS Bandgaps

All bandgaps, including CMOS bandgaps, have the same basic structure: A PTAT current is generated and dropped across a resistor and diode. A common CMOS bandgap generator is shown in the following circuit. The main difference between a BiCMOS and CMOS PTAT current generator is the addition of a NMOS current mirror or operational amplifier to fix the voltage across the PTAT voltage. In the following figure, these MOS devices consist of MN1 and MN2. It is these two devices which greatly reduces the performance of a CMOS bandgap with respect it's BiCMOS counterpart. The mismatches and the noise in the NMOS devices are greatly amplified to the output. For a good untuned bandgap a BiCMOS bandgap will exhibit variations less than 1%, while it's CMOS counterpart exhibits

good unbuffered bandgap a BiCMOS bandgap will exhibit variations less than 1%, while it's CMOS counterpart exhibits variations in the 5% range.

A self-biased cascode CMOS bandgap with start-up circuit is shown in the following figure. The circuit looks complicated and like it will consume much current, because of the many bias legs. In reality the circuit only consumes a small increase increase in current from a regular bandgap, because most of the bias currents are smaller than the core bandgap current.

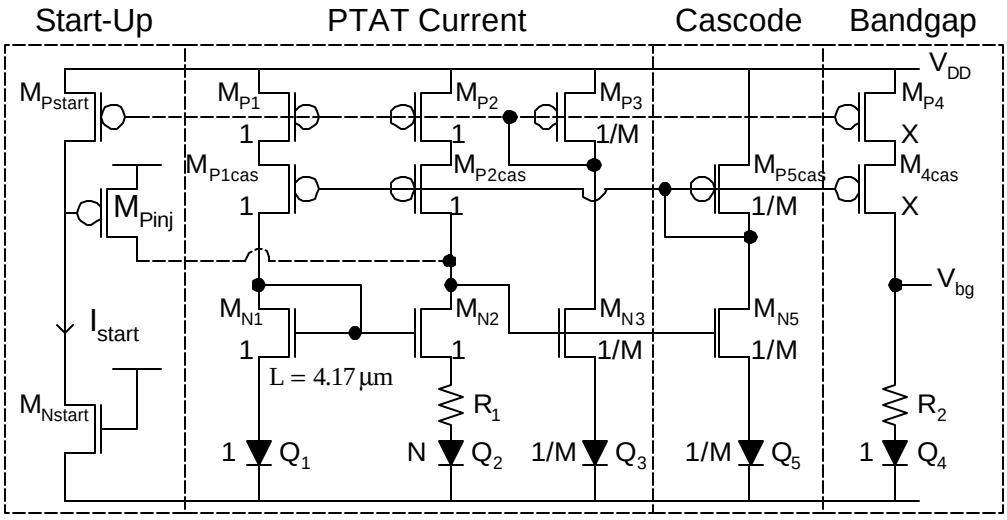


Fig. 1: CMOS bandgap and start-up circuit with low sensitivity to process variations and rout

The noise analysis, bandgap variation analysis, and device sizing routines are nearly identical to the circuit without cascodes. The cascode devices are sized identically to the PMOS current mirror devices, and the cascode bias generator is sized 1/4 the size the other PMOS devices.

The design procedure for CMOS bandgaps is similar to that of BiCMOS bandgaps:

1. Size V_{DSsat}s for headroom constraints.
2. Size the current for thermal leaving a 3dB budget for 1/f noise.
3. Size the MOS lengths for 1/f noise
4. Size BJT area, resistor widths, and MOS lengths for matching.
5. Size MOS widths.
6. Size capacitors for stability if necessary

Thus we begin the design procedure by finding the headroom constraints.

CMOS Bandgap

CMOS BG Headroom Constraints

CMOS Bandgap Headroom Constraints

The sizing of the CMOS bandgap begins with the DC biasing constraints. First we make the NMOS V_{DSsatN} as low as possible to minimize thermal and 1/f noise.

$V_{DSsatN} := 100mV$

The PMOS cascodes are sized near minimum to maximum headroom.

$V_{DSsatPcas} := 0.15V$

The lengths of the PMOS cascodes are sized to a minimum to save area. This has negligible impact on 1/f noise and variation in the bandgap voltage.

$L_{Pcas} := L_{min}$

The bipolar transistor ratio, N, is sized a convenient ratio for layout: 3, 8, 24. Increasing N results in an exponential increase in area for a linear improvement in noise. A good compromise of area and power is an N of 8. Changing from N=8 to N=24 will increase the area by 300% for only a 33% reduction in power.

$N = 8$

We make the current mirror ratios for the bias circuits just large enough to make the currents negligible.

$S = 5$ $M := 4$

The PTAT current is mirrored to the bandgap increased by a factor of X. Increasing the factor X reduces the thermal noise, which indirectly allows current to be reduced, but directly increases the power dissipation. Decreasing X increases resistor area and decreased MOSFET area slightly. X can be optimized to save power, but here we choose a value of 1 for simplicity.

$X = 1$

The V_{DSsat}'s of the PMOS current mirror transistors are sized as large as possible under the worst case scenario, to minimize noise and improve matching for a given area.

$V_{DSsatP1} := V_{DDmin} - V_{BEmax} - V_{DSsatN} - V_{TNmax} - V_{DSsatPcas}$

$V_{DSsatP1} = 0.85\,V$

$V_{DSsatP2} := V_{DDmin} - V_{BEmax} - V_{DSsatN} - V_{TPmax}$

$V_{DSsatP2} = 0.9\,V$

$V_{DSsatP} := \min((V_{DSsatP1} \quad V_{DSsatP2}))$

The minimum supply voltage is found using minimum V_{DSsat}s for the worst case bias leg.

$V_{DDbgmin1} := V_{bgmax} + V_{DSsatmin} + V_{DSsatmin}$ $V_{DDbgmin1} = 1.73\,V$

$V_{DDbgmin2} := V_{TPmax} + V_{DSsatmin} + V_{DSsatmin} + V_{DSsatmin} + V_{BE}$ $V_{DDbgmin2} = 2.3\,V$

$V_{DDbgmin3} := V_{DSsatmin} + V_{DSsatmin} + V_{TNmax} + V_{DSsatmin} + V_{BE}$ $V_{DDbgmin3} = 2.2\,V$

$V_{DDbgmin} := \max((V_{DDbgmin1} \quad V_{DDbgmin2} \quad V_{DDbgmin3}))$ $V_{DDbgmin} = 2.3\,V$

CMOS BG Headroom Constraints

Noise of Improved CMOS Bandgap

Noise Analysis of CMOS Bandgap with Improved Sensitivity to Rout

Once we know the headroom constraints, the required current is calculated to meet the noise constraints. This begins by performing a small signal analysis of the circuit. As with the BiCMOS bandgap there are four equations and four unknowns.

$$v_1 = -g_{mMP1}\cdot(v_2 + v_{nMP1})\cdot\left(\frac{1}{g_{mMN1}} + \frac{1}{g_{mQ1}} + R_1\right) + v_{nMN1} + v_{nR1} + v_{nQ1}$$

$$v_2 = -g_{mMN3}\cdot(v_3 + v_{nMN3})\cdot\frac{1}{g_{mMP3}} + v_{nMP3}$$

$$v_3 = -\left[g_{mMP2}\cdot(v_2 + v_{nMP2}) + \frac{g_{mMN2}}{1 + g_{mMN2}\cdot\frac{1}{g_{mQ2}}}\cdot(v_1 + v_{nMN2} + v_{nQ2})\right]\cdot R_o$$

Simplify and solving for v_2, which will be used to solve for v_{bg}:

$$v_2^2 = \frac{2}{(g_{mMP1}\cdot R_1)^2}\cdot v_{nMN1}^2 + \left[\frac{\left(1 + \frac{g_{mQ1}}{g_{mMN1}}\right)^2}{(R_1\cdot g_{mQ1})^2} + \frac{\left(R_1\cdot g_{mQ1} + \frac{g_{mQ1}}{g_{mMN1}} + 1\right)^2}{(R_1\cdot g_{mQ1})^2}\right]\cdot v_{nMP1}^2 + \frac{2\cdot v_{nQ1}^2}{(g_{mMP1}\cdot R_1)^2} + \frac{v_{nR1}^2}{(g_{mMP1}\cdot R_1)^2}$$

This is simplified with the following variable substitutions:

$$g_{mQ1} = g_m = \frac{I}{V_T} \qquad v_{nQ1}^2 = v_{nQ2}^2 = 4\cdot k\cdot Temp\cdot\frac{V_T}{2\cdot I} \qquad v_{nR1}^2 = 4\cdot k\cdot Temp\cdot\frac{V_T\cdot\ln(N)}{I}$$

$$R_1 = \frac{V_T \cdot \ln(N)}{I} \qquad g_{mMN1} = \frac{2 \cdot I}{V_{DSsatN}} \qquad v_{nMN1}^2 = 4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot \frac{2 \cdot I}{V_{DSsatN}}}$$

$$g_{mMP1} = \frac{2 \cdot I}{V_{DSsatP}} \qquad v_{nMP1}^2 = 4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot \frac{2 \cdot I}{V_{DSsatP}}}$$

$$v_2^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T}{I \cdot \ln(N)^2} \cdot \left(\frac{V_{DSsatP}}{V_T} \right)^2 \cdot \left[\frac{V_{DSsatN}}{6 \cdot V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1 \right)^2 \right] \cdot \frac{V_T}{3 \cdot V_{DSsatP}} + \frac{1 + \ln(N)}{4} \right]$$

Now applying v_2^2 to find the output noise:

$$v_n^2 = \left(v_2^2 + v_{nMP4}^2 \right) \cdot g_{mMP4}^2 \cdot \left(R_2 + \frac{1}{g_{mQ4}} \right)^2 + v_{nR2}^2 + v_{nQ4}^2$$

Making the following variable substitutions:

$$\frac{R_2}{R_1} = \frac{K_{ptat}}{X \cdot \ln(N)} \qquad g_{mMP4} = \frac{2 \cdot I \cdot X}{V_{DSsatP}} \qquad v_{nMP4}^2 = 4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot \frac{2 \cdot I \cdot X}{V_{DSsatP}}}$$

$$v_{nR2}^2 = 4 \cdot k \cdot Temp \cdot R_2 \qquad v_{nQ4}^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T}{2 \cdot I \cdot X} \qquad g_{mQ4} = \frac{I \cdot X}{V_T}$$

$$v_{bg}^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T}{v_n^2} \cdot \left[\left[\frac{2}{3} \cdot \frac{V_{DSsatN}}{V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1 \right)^2 \right] \cdot \frac{4}{3} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \ldots \right] \cdot \frac{1}{\ln(N)^2} \cdot \left(\frac{V_{bg} - V_{BE0}}{V_T} \right. \right.$$
$$\left. \left. + 1 + \ln(N) + \frac{4 \cdot \ln(N)^2}{3 \cdot X} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \right] \right.$$

Assuming V_{bg}-V_{BE0}>>V_T, the bandgap noise can be expressed as:

$$v_{bg}^2 = 4 \cdot k \cdot Temp \cdot \frac{V_T}{v_n^2} \cdot \left[\left[\frac{2}{3} \cdot \frac{V_{DSsatN}}{V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1 \right)^2 \right] \cdot \frac{4}{3} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \ldots \right] \cdot \frac{1}{\ln(N)^2} \cdot K_{ptat}^2 + \frac{K_{pta}}{X} \right.$$
$$\left. + 1 + \ln(N) + \frac{4 \cdot \ln(N)^2}{3 \cdot X} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \right] \right]$$

Solving for current, I

$$I = 4 \cdot k \cdot Temp \cdot \frac{V_T}{v_n^2} \cdot \left[\left[\frac{2}{3} \cdot \frac{V_{DSsatN}}{V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1 \right)^2 \right] \cdot \frac{4}{3} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \ldots \right] \cdot \frac{1}{\ln(N)^2} \cdot (K_{ptat} + 1)^2 + \frac{K_{}}{}$$
$$\left. + 1 + \ln(N) + \frac{4 \cdot \ln(N)^2}{3 \cdot X} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \right] \right]$$

Repeating the noise derivation for 1/f noise alone we get

$$v_{bg1\_f}^2 = g_{mMP4}^2 \cdot \left(R_2 + \frac{1}{g_{mQ4}} \right)^2 \cdot \left[v_{nMP4}^2 + \frac{2 \cdot v_{nMN1}^2}{(g_{mMP1} \cdot R_1)^2} + \left[\frac{\left(1 + \frac{g_{mQ1}}{g_{mMN1}} \right)^2}{(R_1 \cdot g_{mQ1})^2} + \frac{\left(R_1 \cdot g_{mQ1} + \frac{g_{mQ1}}{g_{mMN1}} + 1 \right)^2}{(R_1 \cdot g_{mQ1})^2} \right] \cdot v_{nMP1}^2 \right]$$

Usually 1/f noise is dominated by NMOS transistors. Dropping the PMOS noise terms and substituting in expressions for the NMOS the bandgap noise becomes.

$$v_{nMN1}^2 = \frac{K_{fN}}{W \cdot L \cdot f} \qquad W_N = \frac{2 \cdot I \cdot L}{\mu N C O X \cdot V_{DSsatN}^2}$$

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$$v_{bg1\_f}^2 = \left(\frac{K_{ptat}}{\ln(N)} + \frac{\frac{V_{DSsatP}}{2}}{V_T \cdot \ln(N)} \right) \cdot \frac{K_{fN} \cdot \mu NCOX \cdot V_{DSsatN}^2}{I \cdot L_N^2 \cdot f}$$

Here we see we can size L, given noise and current, or size current given noise and L. Increasing L saves current and increasing current saves area, but on the lower limit current is constrained by thermal noise. The required length to meet noise requirements are:

$$L_N = \left(\frac{K_{ptat}}{\ln(N)} + \frac{\frac{V_{DSsatP}}{2}}{V_T \cdot \ln(N)} \right)^2 \cdot \frac{K_{fN} \cdot \mu NCOX \cdot V_{DSsatN}^2}{v_{bg1\_f}^2 \cdot L_N^2 \cdot f}$$

From this derivation of the bandgap noise, we see that for large R_{out} the noise of the this bandgap is exactly the same as a simpler bandgap, where the PMOS current is simply mirrored instead of being passed through a high-gain circuit. A simplified formula to quickly estimating bandgap noise from a given current is given below:

$$v_n^2 = 4 \cdot k \cdot Temp \cdot R_2 \cdot \frac{R_2}{R_1} = 4 \cdot k \cdot Temp \cdot \frac{V_T \cdot \ln(N)}{I} \cdot 20^2$$

Noise of Improved CMOS Bandgap

CMOS Bandgap Area

CMOS Bandgap Area

Equations for the area of the CMOS bandgap and start-up circuits are important for optimization. The area takes the following form:

$$Area = 2 \cdot W_N \cdot (L_N + 2 \cdot L_{min}) + \left(2 + X + \frac{1}{M} + \frac{1}{S}\right) \cdot W_P \cdot (L_P + 2 \cdot L_{min}) + (N + 1) \cdot Area \cdot Q_1 + W_R \cdot (L_{R1} + L_{R2} + L_{min}) \ldots + (L_{start} + 2 \cdot L_{min}) \cdot W_{start}$$

If the circuit is cascoded the area becomes:

$$Area = 2 \cdot W_N \cdot (L_N + 2 \cdot L_{min}) + \left(2 + X + \frac{1}{M} + \frac{1}{S}\right) \cdot \left[W_P \cdot (L_P + 2 \cdot L_{min}) + W_{Pcas} \cdot (L_{Pcas} + 2 \cdot L_{min})\right] + (N + 1) \cdot Area \cdot Q_1 \ldots + W_R \cdot \left(\frac{W_R}{R_{sq}} \cdot \frac{V_T \cdot \ln(N)}{I} + \frac{W_R}{R_{sq}} \cdot \frac{R_2}{R_1} \cdot \frac{V_T \cdot \ln(N)}{I} + L_{min} \right) + (L_{start} + 2 \cdot L_{min}) \cdot W_{start}$$

Making variable substitutions and simplifying to only active area

$$W_N = \frac{2 \cdot I \cdot L_N}{\mu NCOX \cdot V_{DSsatN}^2} \qquad W_P = \frac{2 \cdot I \cdot L_P}{\mu NCOX \cdot V_{DSsatP}^2} \qquad W_{Pcas} = \frac{2 \cdot I \cdot L_{Pcas}}{\mu NCOX \cdot V_{DSsatPcas}^2} \qquad L_{R1} = \frac{W_R}{R_{sq}} \cdot R_1 = \frac{W_R}{R_{sq}} \cdot \frac{V_T \cdot \ln(N)}{I}$$

$$L_{R2} = \frac{W_R}{R_{sq}} \cdot R_2 = \frac{W_R}{R_{sq}} \cdot \frac{R_2}{R_1} \cdot \frac{V_T \cdot \ln(N)}{I}$$

The area becomes

$$Area = 2 \cdot \frac{2 \cdot I \cdot L_N^2}{\mu NCOX \cdot V_{DSsatN}^2} + \left(2 + X + \frac{1}{M} + \frac{1}{S}\right) \cdot \left(\frac{2 \cdot L_P^2}{\mu NCOX \cdot V_{DSsatP}^2} + \frac{2 \cdot L_{Pcas}^2}{\mu NCOX \cdot V_{DSsatPcas}^2} \right) \cdot I + (N + 1) \cdot Area \cdot Q_1 \ldots + W_R \cdot (L_{R1} + L_{R2} + L_{min}) + (L_{start} + 2 \cdot L_{min}) \cdot W_{start}$$

CMOS Bandgap Area

CMOS Bandgap Current Sizing

The length of the PMOS transistors are sized to improve the matching of the PMOS current mirrors and thus reduce the variance of the output voltage. The sizing requires the knowledge of the current. So a a first guess at the

reduce the variance of the output voltage. The sizing requires the knowledge of the current. So we first guess at the length and size the current, then later go back and size the current appropriately for matching. The same logic applies to the width of the resistors.

$L_P := 2 \cdot L_{min}$

$W_R := W_{min}$

A common coefficient for bandgap design is the R_2/R_1 ratio, which largely is fixed by the process, but varies somewhat with V_{BE0}, which varies with device size and current.

$$R2\_R1 := \frac{K_{ptat}}{X \cdot \ln(N)} \qquad R2\_R1 = 9.84$$

With the bandgap above the area coefficients become:

$$Area = A_{LI} \cdot L^2 \cdot I + A_I \cdot I + \frac{A_R}{I} + A_0$$

$$A_{LI} := \frac{2}{\mu_N \cdot C_{OX} \cdot V_{DSsatN}^2} \qquad A_{LI} = 4.51 \frac{\mu m^2}{\mu m^2 \cdot \mu A}$$

$$A_I := \left(2 + X + \frac{1}{M} + \frac{1}{S}\right) \cdot \left[\frac{2 \cdot L_P}{\mu_N \cdot C_{OX} \cdot V_{DSsatP}^2} \cdot (L_P + 2 \cdot L_{min}) + \frac{2 \cdot L_{Pcas}}{\mu_N \cdot C_{OX} \cdot V_{DSsatPcas}^2} \cdot (L_{Pcas} + 2 \cdot L_{min})\right] \qquad A_I = 5.62 \frac{\mu m^2}{\mu A}$$

$$A_R := \frac{W_R^2}{R_{sq}} \cdot V_T \cdot \ln(N) \cdot (1 + R2\_R1) \qquad A_R = 302.25\,\mu m^2 \cdot \mu A$$

The power coefficients become

$$Power = P_I \cdot I + P_0$$

$$P_I := V_{DD} \cdot \left(2 + X + \frac{2}{M} + \frac{1}{S}\right) \qquad P_0 := 0$$

The noise coefficients become

$$P_I = 11.1 \frac{mW}{mA}$$

$$Noise = \frac{N_{LI}}{L^2 \cdot I} + \frac{N_I}{I} + N_0$$

$$N_{LI} := \left(\frac{K_{ptat}}{\ln(N)} + \frac{\frac{V_{DSsatP}}{2}}{V_T \cdot \ln(N)}\right)^2 \cdot \frac{K_{fN} \cdot \mu_N \cdot C_{OX} \cdot V_{DSsatN}^2}{f} \qquad N_{LI} = 0\,kg^2\,m^6\,s^{-5}\,A^{-1}$$

$$N_I := 4 \cdot k \cdot Temp \cdot V_T \cdot \left[\left[\frac{2}{3} \cdot \frac{V_{DSsatN}}{V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T}\right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1\right)^2\right] \cdot \frac{4}{3} \cdot \left(\frac{V_T}{V_{DSsatP}}\right) \ldots\right] \cdot \frac{1}{\ln(N)^2} \cdot (K_{ptat} + 1)^2 + \ldots\right.$$

$$\left. + 1 + \ln(N) + \frac{4 \cdot \ln(N)^2}{3 \cdot X} \cdot \left(\frac{V_T}{V_{DSsatP}}\right)\right]$$

$$N_0 := 0 \frac{V^2}{Hz}$$

The cost coefficients become

$$Cost = C_P \cdot Power + C_A \cdot Area$$

The optimal current assuming thermal noise is negligible is:

$$I_{opt1\_f} := \sqrt{\frac{C_A \cdot A_R}{(C_P \cdot P_I + C_A \cdot A_I)}} \qquad I_{opt1\_f} = 1.33\,\mu A$$

Assuming there are no resistors, A_R=0, the optimal current becomes:

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$$I_{optnores} := \frac{N_I + \sqrt{\frac{C_A \cdot A_{LI} \cdot N_{LI} \cdot N_I}{(C_P \cdot P_I + C_A \cdot A_I)}}}{v_n^2 - N_0} \qquad I_{optnores} = 1.42\,mA$$

Sizing current for optimal area only yields

$$I_{optarea} := \sqrt{\frac{A_R}{A_I}} \qquad I_{optarea} = 7.33\,\mu A$$

Sizing the circuit for cost due to resistor area and power only:

$$I_{optresonly} := \sqrt{C_A \cdot \frac{A_R}{C_P \cdot P_I}} \qquad I_{optresonly} = 1.36\,\mu A$$

Sizing the current for thermal noise alone yields

$$I_{optthermal} := 4 \cdot k \cdot Temp \cdot \frac{V_T}{v_n^2} \cdot \left[\left[\frac{2}{3} \cdot \frac{V_{DSsatN}}{V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1 \right)^2 \right] \cdot \frac{4}{3} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \ldots \right] \cdot \frac{1}{\ln(N)^2} \cdot \left(K_{ptat} \cdot \right. \right.$$
$$\left. \left. + 1 + \ln(N) + \frac{4 \cdot \ln(N)^2}{3 \cdot X} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \right] \right]$$

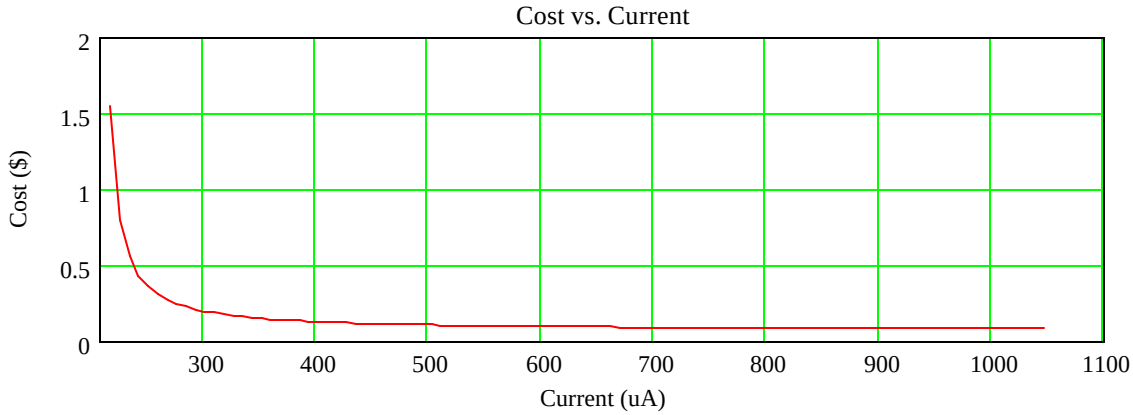
$I_{optthermal} = 0.21\,mA$

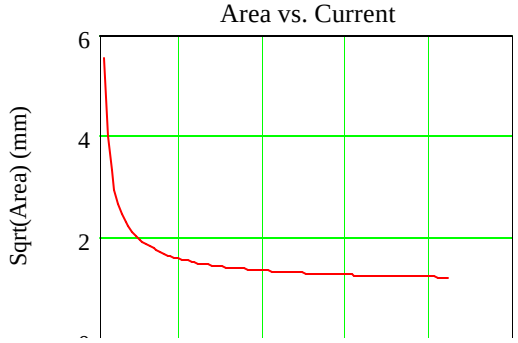
Using a root finder to find the optimal current to minimize cost yields

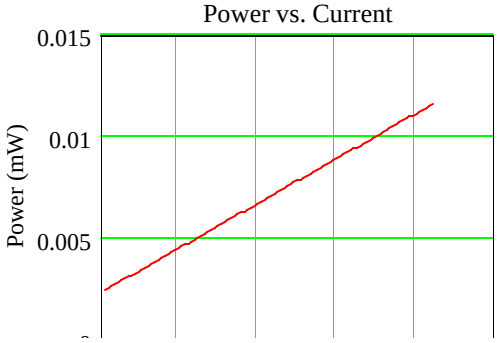
$$I_{opt} := \left| I \leftarrow I_{optthermal} \cdot 2 \right| \qquad I_{opt} = 1.42\,mA$$
$$\left| \text{root}\left[C_P \cdot P_I + C_A \cdot \left[\frac{-A_{LI} \cdot N_{LI} \cdot N_I}{\left[\left(v_n^2 - N_0 \right) \cdot I - N_I \right]^2} + A_I - \frac{A_R}{I^2} \right], I \right]$$

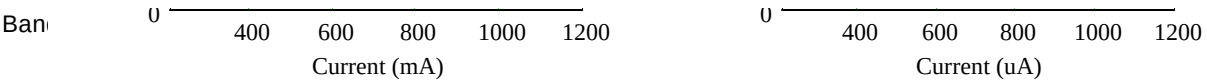
$i := 1 .. num$

$$Ival_i := \frac{i}{num} \cdot 4 \cdot I_{optthermal} + I_{optthermal}$$









We can choose the current, I, based on any of the possible criterion above. From the analysis above we see that we the minimum a current can be is set by the thermal noise. We want to make the

$$I := \begin{cases} I_{optthermal} & \text{if } (Force_I = 0)\cdot(No1\_f = 1) \\ I_{opt} & \text{if } (Force_I = 0)\cdot(No1\_f = 0) \\ I_{force} & \text{if } Force_I = 1 \end{cases} \qquad I = 1.42\,mA$$

$$I := I_{fix}(I) \qquad I = 1.42\,mA$$

With the current known we can find the NMOS length needed to meet 1/f requirements

$$L_{N1\_f} := \left(\frac{K_{ptat}}{\ln(N)} + \frac{\frac{V_{DSsatP}}{2}}{V_T \cdot \ln(N)} \right) \cdot \sqrt{\frac{2 \cdot K_{fN} \cdot \mu_N \cdot C_{OX} \cdot V_{DSsatN}^2}{v_n^2 \cdot I \cdot f}} \qquad L_{N1\_f} = 19.25\,\mu m$$

With the current known the PTAT current setting resistor can be found

$$R_1 := \frac{V_T \cdot \ln(N)}{I} \qquad R_1 = 39.36\,\Omega$$

With the current known the K_{ptat} coefficient must be resized to reflect a more accurate value for V_{BE0}, which is calculated with the actual current used.

$$V_{BE0} := V_T \cdot \ln\left(\frac{I}{I_s}\right) \qquad V_{BE0} = 0.81\,V$$

$$K_{ptat} := \frac{V_{G0} - V_{BE0}}{V_T} + (\gamma - \alpha) \qquad K_{ptat} = 17.51$$

The bandgap resistor, R_2, is sized to null the temperature coefficient. In practice R_2 can be tweaked in the final design to center the temperature coefficient to account for second order affects.

$$R_2 := \left(\frac{K_{ptat}}{\ln(N) \cdot X}\right) \cdot R_1 \qquad R_2 = 0.33\,k\Omega$$

Sometimes the required noise for the bandgap is not known, but must be budgeted from an overall system specification. In this case the system-level optimization requires the following noise coefficient.

$$v_n^2 = \frac{K_{Nbg}}{I}$$

$$K_{Nbg} := 4 \cdot k \cdot Temp \cdot V_T \cdot \left[\left[\frac{2}{3} \cdot \frac{V_{DSsatN}}{V_T} + \left[\left(1 + \frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \left(\ln(N) + \frac{V_{DSsatN}}{2 \cdot V_T} + 1 \right)^2 \right] \cdot \frac{4}{3} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \ldots \right] \cdot \frac{1}{\ln(N)^2} \cdot (K_{ptat} + 1)^2 \right.$$
$$\left. + 1 + \ln(N) + \frac{4 \cdot \ln(N)^2}{3 \cdot X} \cdot \left(\frac{V_T}{V_{DSsatP}} \right) \right]$$

$$K_{Nbg} = 268.25 \frac{nV^2}{Hz} \cdot mA$$

CMOS Bandgap Current Sizing

Sizing for Bandgap Variance

Sizing Device Areas for Matching Requirements and Area Minimization

The bandgap suffers from two sources of variation. The first is from device matching, which can be improved with increased device area. The second source of variation is from process variation, which cannot be adjusted without trimming to an external reference. This process variation, $DV_{process}$, is a lower limit to a specification for the bandgap

Variation.

$\Delta V_{bg} := \sigma_{\Delta Vbg\_Vbg} \cdot V_{bg}$ $\Delta V_{bg} = 38.44\,mV$

$\Delta V_{bg}^2 = \sqrt{\Delta V_{bgprocess}^2 + \Delta V_{bgmismatch}^2}$

$\Delta V_{bgprocess} := V_T \cdot \sqrt{\sigma_{\Delta R\_Rprocess}^2 + \Delta Is\_Is_{process}^2}$ $\Delta V_{bgprocess} = 9.66\,mV$ $\frac{\Delta V_{bgprocess}}{V_{bg}} = 0.75\,\%$

We substract the bandgap variation due to process variations to find the allocation of the desired bandgap variation to the mismatch variation.

$\Delta V_{bgmismatch} := \sqrt{\Delta V_{bg}^2 - \Delta V_{bgprocess}^2}$ $\Delta V_{bgmismatch} = 37.2\,mV$

A detailed derivation of bandgap variance is described in another section.

$$\Delta V_{bgmismatch}^2 = V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \left[\frac{\Delta R\_R^2}{\left(\frac{R_2}{R_1}\right)} + \left[\frac{\Delta Is\_Is^2}{N} + \left[\left(\frac{\Delta L}{L_N}\right)^2 + \left(\frac{\Delta W}{W_N}\right)^2\right] \cdot \left(\frac{V_{DSsatN}}{2 \cdot V_T}\right)^2 + \frac{\Delta V_{thN}^2}{V_T^2}\right] \cdot \frac{1}{\ln(N)^2} \ldots + \Delta I\_I_{mir}^2 \cdot \left[\left(1 + \frac{\frac{V_{DSsat}}{2 \cdot V_T} + 1}{\ln(N)}\right)^2 + \frac{1}{X}\right]\right]$$

Making the following variable substitutions. For the variance in R, first find the variance for minimum width and then use the following expression:

$\Delta R\_R^2 = \frac{\Delta R\_R_{min}^2 \cdot W_{min}^2}{W_R^2}$ Resistor Variation ,where $\Delta R\_R_{min} := \sqrt{\frac{\left(\frac{R_{sq} \cdot \sigma_{\Delta L}}{R_1}\right)^2 + \sigma_{\Delta W}^2}{W_{min}^2}}$ $\Delta R\_R_{min} = 406.77\,\%$

$\sigma_{\Delta VTP}^2 = \Delta V_{thPLmin}^2 \cdot \frac{L_{min}^2}{L_P^2}$ 3σ PMOS Threshold Variation, where

$\Delta V_{thPLmin} := \sqrt{\sigma_{\Delta VTPLmin}^2 \cdot V_{DSsat}^2 \cdot \mu_P \cdot C_{OX} \cdot \frac{20\mu m}{2 \cdot I \cdot L_{min}}}$ $\Delta V_{thPLmin} = 15.57\,mV$

$\sigma_{\Delta VTN}^2 = \Delta V_{thLnmin}^2 \cdot \frac{L_{min}^2}{L_N^2}$ 3σ NMOS Threshold Variation, where

$\Delta V_{thNLmin} := \sqrt{\sigma_{\Delta VTNLmin}^2 \cdot V_{DSsat}^2 \cdot \mu_N \cdot C_{OX} \cdot \frac{20\mu m}{2 \cdot I \cdot L_{min}}}$ $\Delta V_{thNLmin} = 22.18\,mV$

$\sigma_{\Delta I\_I.mir} = \sqrt{\Delta V_{thPLmin}^2 \cdot \frac{L_{min}^2}{L_P^2} \cdot \left(\frac{2}{V_{DSsatP}}\right)^2 + \sigma_{\Delta W}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}{2 \cdot I \cdot L_P}\right)^2 + \frac{\sigma_{\Delta L}^2}{L_P^2}}$ Current Mirror Mismatch

$\sigma_{\Delta Is\_Is}^2 = \sigma_{\Delta Is\_IsAreamin}^2 \cdot \frac{Area_{Q1min}}{Area_{Q1}}$ Bipolar Transistor Reverse Saturation Current Mismatch

$W_N = \frac{2 \cdot I \cdot L_N}{\mu_N \cdot C_{OX} \cdot V_{DSsatN}^2}$

The bandgap variance expression becomes

$$\Delta V_{bgmismatch}^2 = V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \left[\frac{\Delta R\_R_{min}^2 \cdot W_{min}^2}{\frac{R_2}{R_1} \cdot W_R^2} \ldots\right.$$

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$$\left| + \left[\frac{\Delta Is\_Is_{Areamin}{}^2}{N} \cdot \frac{Area_{min}}{Area_{Q1}} + \left[\left(\frac{\Delta L}{L_N} \right)^2 + \left(\frac{\Delta W \cdot \mu_N \cdot C_{OX} \cdot V_{DSsatN}{}^2}{2 \cdot I \cdot L_N} \right) \right] \cdot \left(\frac{V_{DSsatN}}{2 \cdot V_T} \right.\right.$$

$$\left. + \left[\Delta V_{thPLmin}{}^2 \cdot \frac{L_{min}{}^2}{L_P{}^2} \cdot \left(\frac{2}{V_{DSsatP}} \right)^2 + \sigma_{\Delta W}{}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}{}^2}{2 \cdot I \cdot L_P} \right)^2 + \frac{\sigma_{\Delta L}{}^2}{L_P{}^2} \right] \cdot \left[\left(1 + \right. \right. \right.$$

The expression for the bandgap mismatch can be simplified to:

$$\Delta V_{bgmismatch}{}^2 = \frac{X_1}{W_R{}^2} + \frac{X_2}{Area_{Q1}} + \frac{X_3}{L_N{}^2} + \frac{X_4}{L_P{}^2}$$

where

$$X_1 := V_T{}^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1 \right)^2 \cdot \frac{\Delta R\_R_{min}{}^2 \cdot W_{min}{}^2}{\left(\frac{R_2}{R_1} \right)} \qquad \sqrt{X_1} = 695.6\,mV \cdot \mu m$$

$$X_2 := V_T{}^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1 \right)^2 \cdot \frac{1}{\ln(N)^2} \cdot \frac{\sigma_{\Delta Is\_IsAreamin}{}^2}{N} \cdot Area_{BJTmin} \qquad \sqrt{X_2} = 18.87\,mV \cdot \mu m$$

$$X_3 := V_T{}^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1 \right)^2 \cdot \frac{1}{\ln(N)^2} \cdot \left[\left[\sigma_{\Delta L}{}^2 + \left(\frac{\sigma_{\Delta W} \cdot \mu_N \cdot C_{OX} \cdot V_{DSsatN}{}^2}{2 \cdot I} \right)^2 \right] \cdot \left(\frac{V_{DSsatN}}{2 \cdot V_T} \right)^2 + \frac{\sigma_{\Delta VTNLmin}{}^2}{V_T{}^2} \cdot L_{min}{}^2 \right]$$

$$\sqrt{X_3} = 60.91\,mV \cdot \mu m$$

$$X_4 := V_T{}^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1 \right)^2 \cdot \left[\left[\sigma_{\Delta VTPLmin}{}^2 \cdot L_{min}{}^2 \cdot \left(\frac{2}{V_{DSsatP}} \right)^2 \ldots \right.\right.$$

$$\left.\left. + \sigma_{\Delta W}{}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}{}^2}{2 \cdot I} \right)^2 + \sigma_{\Delta L}{}^2 \right] \cdot \left[\left(1 + \frac{\frac{V_{DSsat}}{2 \cdot V_T} + 1}{\ln(N)} \right)^2 + \frac{1}{X} \right] \right]$$

$$\sqrt{X_4} = 967.77\,mV \cdot \mu m$$

The area for the circuit expressed as a function of the variables above is derived in an earlier section:

$$Area = 2 \cdot \frac{2 \cdot I \cdot L_N{}^2}{\mu NCOX \cdot V_{DSsatN}{}^2} + \left(2 + X + \frac{1}{M} + \frac{1}{S} \right) \cdot \left(\frac{2 \cdot I \cdot L_P \cdot L_P}{\mu NCOX \cdot V_{DSsatP}{}^2} + W_{Pcas} \cdot L_{Pcas} \right) + \left(N + 1 + \frac{1}{M} \right) \cdot Area \cdot Q_1 \ldots$$

$$+ W_R \cdot \left(\frac{W_R}{R_{sq}} \cdot \frac{V_T \cdot \ln(N)}{I} + \frac{W_R}{R_{sq}} \cdot \frac{R_2}{R_1} \cdot \frac{V_T \cdot \ln(N)}{I} \right) + L_{start} \cdot W_{start}$$

The active area can be expressed as the following simplified form:

$$Area = Y_1 \cdot W_R{}^2 + Y_2 \cdot Area_{Q1} + Y_3 \cdot L_N{}^2 + Y_4 \cdot L_P{}^2$$

$$Y_1 := \frac{1}{R_{sq}} \cdot \frac{V_T \cdot \ln(N)}{I} + \frac{1}{R_{sq}} \cdot \frac{R_2}{R_1} \cdot \frac{V_T \cdot \ln(N)}{I} \qquad Y_1 = 0.19\,\frac{\mu m}{\mu m}$$

$$Y_2 := \left(N + 1 + \frac{1}{M} \right) \qquad Y_2 = 9.25\,\frac{\mu m}{\mu m}$$

$$Y_3 := 2 \cdot \frac{2 \cdot I}{\mu_N \cdot C_{OX} \cdot V_{DSsatN}{}^2} \qquad Y_3 = 1.28 \times 10^4\,\frac{\mu m}{\mu m}$$

$$Y_4 := \left(2 + X + \frac{1}{M} + \frac{1}{S} \right) \cdot \frac{2 \cdot I}{\mu_N \cdot C_{OX} \cdot V_{DSsatP}{}^2} \qquad Y_4 = 305.26\,\frac{\mu m}{\mu m}$$

Using the equations above to minimize active area, we get the following solutions for the device widths:

Using the equations above to minimize active area, we get the following solutions for the device widths:

$$Area_{opt} := \frac{\left(\sqrt{Y_1 \cdot X_1} + \sqrt{Y_2 \cdot X_2} + \sqrt{Y_3 \cdot X_3} + \sqrt{Y_4 \cdot X_4}\right)^2}{\Delta V_{bgmismatch}^{\ 2}}$$

Minimum Total Area

$$\sqrt{Area_{opt}} = 649.26\,\mu m$$

$$Area_{Q1} := \sqrt{\frac{Area_{opt}}{\Delta V_{bgmismatch}^{\ 2}} \cdot \frac{X_2}{Y_2}}$$

Optimum Bipolar Transistor Area to Minimize Total Area

$$\sqrt{Area_{Q1}} = 10.41\,\mu m$$

$$L_N := \sqrt{\sqrt{\frac{Area_{opt}}{\Delta V_{bgmismatch}^{\ 2}} \cdot \frac{X_3}{Y_3}}}$$

Optimum NMOS Length to Minimize Total Area

$$L_N = 3.07\,\mu m$$

$$L_P := \sqrt{\sqrt{\frac{Area_{opt}}{\Delta V_{bgmismatch}^{\ 2}} \cdot \frac{X_4}{Y_4}}}$$

Optimum PMOS Length to Minimize Total Area

$$L_P = 31.09\,\mu m$$

$$W_R := \sqrt{\sqrt{\frac{Area_{opt}}{\Delta V_{bgmismatch}^{\ 2}} \cdot \frac{X_1}{Y_1}}}$$

Optimum Resistor Width to Minimize Total Area

$$W_R = 167.9\,\mu m$$

The lengths, widths, and areas are constrained by specified values or on the lower limit by L_{min} and Wmin.

$Area_{Q1} := Area_{fix}(Area_{Q1})$ $\quad \sqrt{Area_{Q1}} = 10.41\,\mu m$

$L_N := L_{fix}(L_N)$ $\quad L_N = 2\,\mu m$

$L_P := L_{fix}(L_P)$ $\quad L_P = 2\,\mu m$

$W_R := W_{fix}(W_P)$ $\quad W_R = 1.7\,\mu m$

In practice we want to minimize total area instead of active area, but this method allows simple closed form solutions, which serve as excellent estimates of the optimal solution, while maintaining variance goal objectives.

$$\Delta V_{bgmismatch}^{\ 2} = \frac{K_{mismatchbg}}{Area_{bg}} \qquad K_{mismatchbg} := \left(\sqrt{Y_1 \cdot X_1} + \sqrt{Y_2 \cdot X_2} + \sqrt{Y_3 \cdot X_3}\right)^2 \qquad \sqrt{K_{mismatchbg}} = 7.24\,mV \cdot mm$$

Sizing for Bandgap Variance

Device Sizing

Sizing Other Device Dimensions

$$I = \frac{V_T \cdot \ln(N)}{R_1 \cdot (1 + \Delta R\_R)} \qquad I_{min} = \frac{V_T \cdot \frac{Temp_{min}}{Temp} \cdot \ln(N)}{R_1 \cdot (1 + \Delta R\_R)} = I \cdot (1 - \Delta I\_I)$$

Where ΔR_R is used to indicate variations in the absolute process and not in matching. Assuming T_0 is centered around the maximum and minimum operating temperatures the variance in the temperature and the PTAT current are:

$$\sigma_{\Delta I\_I} := \sqrt{\sigma_{\Delta R\_Rprocess}^{\ 2} + \sigma_{\Delta Temp\_Te}} \qquad \sigma_{\Delta I\_I} = 29.54\,\%$$

Once the current is known we can size the rest of the device dimensions. The width of the PMOS transistors can be sized to meet the current and V_{DSsat} requirements. We use the minimum device transconductance and the maximum current for sizing the device to model worst case operating conditions. The PMOS cascode devices are sized similarly.

$$W_P := \frac{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I}) \cdot L_P}{\mu PCOXmin \cdot V_{DSsatP}^{\ 2}} \qquad W_P = 373.87\,\mu m$$

$2 \cdot I \cdot (1 + \sigma$ [illegible] $) \cdot L$

Ba $W_{Pcas} := \frac{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I}) \cdot L_{Pcas}}{\mu PCOXmin \cdot V_{DSsatPcas}^{2}}$ $W_{Pcas} = 3\,mm$

The NMOS length is sized from an equation for noise derived in the optimization section

$$L_N := \begin{cases} L_N & \text{if } No1\_f = 1 \\ \sqrt{\frac{N_{LI}}{\left(v_n^2 - N_0\right) \cdot I - N_I}} & \text{if } No1\_f = 0 \end{cases} \qquad L_N = 14.74\,\mu m$$

$L_N := L_{fix}(L_N)$

The NMOS width is sized from it's length, current, and V_{DSsat}.

$W_N := \frac{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I}) \cdot L_N}{\mu NCOXmin \cdot V_{DSsatN}^{2}}$ $W_N = 20.7\,mm$

Given the PTAT current setting resistor value and width, the length can be found:

$L_{R1} := \frac{W_R}{R_{sq}} \cdot R_1$ $L_{R1} = 0.03\,\mu m$

The devices widths and lengths are constrained on the lower limits by W_{min} and Lmin. Here the device sizes are resized based on those constraits. The lower limit on the width constraint affects the bias circuit first. If we fix the bias width constraint first it will automatically correct the width constraint on the main circuit.

$W_P := W_{fix}(W_P)$ $W_P = 373.9\,\mu m$

$L_P := \frac{W_P \cdot \mu PCOXmin \cdot V_{DSsatP}^{2}}{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I})}$ $L_P = 2\,\mu m$

$W_{Pcas} := W_{fix}(W_{Pcas})$

$L_{Pcas} := \frac{W_{Pcas} \cdot \mu PCOXmin \cdot V_{DSsatPcas}^{2}}{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I})}$ $L_{Pcas} = 0.5\,\mu m$

$W_N := W_{fix}(W_N)$ $W_N = 20.7 \times 10^{3}\,\mu m$

$L_N := \frac{W_N \cdot \mu NCOXmin \cdot V_{DSsatN}^{2}}{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I})}$ $L_N = 2\,\mu m$

$L_{R1} := L_{fix}(L_{R1})$ $L_{R1} = 2\,\mu m$

$W_R := \frac{L_{R1} \cdot R_{sq}}{R_1}$ $W_R = 101.62\,\mu m$

Sizing the Bias Generator

The bias transistors for the PMOS current mirror and cascode generator are sized with currents M times lower to save current. Thus the device widths are also M times lower. In practice, to improve matching, the width is not made M times larger for the main device, but instead M devices are used in parallel, each with the same width as the smaller device. The V_{DSsat} of the cascode generator is the sum of the V_{DSsat}s of the cascode and the current mirror.

$I_{bias} := \frac{I}{M}$ $I_{bias} = 354.03\,\mu A$

$L_{Pcasbias} := L_{Pcas}$ $L_{Pcasbias} = 0.5\,\mu m$

$W_{Pcasbias} := \frac{2 \cdot I \cdot (1 + \sigma_{\Delta I\_I}) \cdot L_{Pcas}}{M \cdot \mu PCOXmin \cdot (V_{DSsatP} + V_{DSsatPcas})^{2}}$ $W_{Pcasbias} = 16.88\,\mu m$

$L_{Pbias} := L_P$ $L_{Pbias} = 2\,\mu m$

$W_{Pbias} := \frac{W_P}{M}$ $W_{Pbias} = 93.47\,\mu m$

W_N

Ba $W_{Nbias} := \frac{W_N}{M}$ nd Analysis $W_{Nbias} = 5.18 \times 10^{} \mu m$

$L_{Nbias} := L_N$ $L_{Nbias} = 2\,\mu m$

Sizing the Bandgap Generator

The bandgap resistor, R_2, value and width known we can size the length. There is a length constraint on the resistor but this is limit occurs first for the PTAT current setting resistor, so the bandgap resistor, R2, should be fine.

$L_{R2} := \frac{W_R}{R_{sq}} \cdot R_2$ $L_{R2} = 16.85\,\mu m$

Similarly to the bias transistors the currrent to the bandgap generator is sized X times larger. Thus the device widths are also X times larger. In practice, to improve matching, the width is not made X times larger , but instead X devices are used in parallel, each with the same width as the smaller device.

$W_{Pbg} := X \cdot W_P$ $W_{Pbg} = 373.9\,\mu m$

$L_{Pbg} := L_P$ $L_{Pbg} = 2\,\mu m$

$W_{Pbgcas} := X \cdot W_{Pcas}$ $W_{Pbgcas} = 3\,mm$

$L_{Pbgcas} := L_{Pcas}$ $L_{Pbgcas} = 0.5\,\mu m$

$I_{bg} := X \cdot I$ $I_{bg} = 1.42 \times 10^{3}\,\mu A$

Sizing the start-up circuit

The start-up current, I_{start}, should be sized less than the main bandgap current to save power. For this reason we size ratio S to be about five.

$I_{Pstart} := \frac{I}{S}$ $I_{Pstart} = 283.22\,\mu A$

$L_{Pstart} := L_P$ $L_{Pstart} = 2\,\mu m$

$W_{Pstart} := \frac{W_P}{S}$ $W_{Pstart} = 74.78\,\mu m$

A lower limit constraint on the width of the start-up device occurs for very low current. At this low current, the current saving from a large current mirror ratio is less important, so the sizing for S can be reduced.

$S := if\left(W_{Pstart} < W_{min}, floor\left(\frac{W_{Pstart}}{W_{min}}\right), S\right)$ $S = 5$

$W_{Pstart} := \frac{W_P}{S}$ $W_{Pstart} = 74.78\,\mu m$

$I_{Pstart} := \frac{I}{S}$ $I_{Pstart} = 2.83 \times 10^{-4}\,A$

The start-up current which flows through the NMOS start-up transistor, M_{Nstart}, must be sized lower than PTAT current divided by S. This allows the start-up transistor to turn off when the circuit is in desired operation. A large safety margin of a factor of 3 under worst case scenarios is used to size this NMOS current. We assume the PMOS start up transistor is deep in the triode region. The worst case scenario is maximum V_{DD}, fast process, low current, which occurs at low temperature.

$I_{Nstart} = \frac{I_{Pstartmin}}{3} = \frac{I_{PTATmin}}{3 \cdot S} = \frac{\mu_{NCOXmax}}{2} \cdot \frac{W_{Nstart}}{L_{Nstart}} \cdot \left(V_{DDmax} - V_{TNmin}\right)^2$ tart $:= \frac{I_{Pstart}}{3}$ $I_{Nstart} = 94.41\,\mu A$

$W_{Nstart} := W_{min}$ $W_{Nstart} = 1\,\mu m$

$L_{Nstart} := \frac{3 \cdot S \cdot \mu NCOXmax}{2 \cdot I \cdot \left(1 - \sigma_{\Delta I\_I}\right)} \cdot W_{Nstart} \cdot \left(V_{DDmax} - V_{TNmin}\right)^2$ $L_{Nstart} = 3.13\,\mu m$

Device Sizing

Phase Margin and Compensation

Phase Margin and the Compensation Capacitor

Stabilizing the bandgap not only requires the negative loop gain to to be greater than the positive loop gain, it also requires positive phase margin at the unity-gain bandwidth of the circuit. In the following section we will discuss the open-loop gain and how to size a compensation capacitor for the circuit to insure a desired phase margin.

There are three potential places to put the compensation capacitor in this circuit. The first is with a capacitor to ground from the high impedance node, V_3. The second place is from the gate to the drain of M_{N2}, which takes advantage of the Miller effect. At first, it appears the Miller affect only applies to the negative feedback path, means at higher frequencies the positive feedback gain will be higher making the circuit unstable. In reality the capacitor , which reduces the impedance of the high-impedance node, reduces the gain of both paths. The third place to put the capacitor is from the gate to drain of M_{P2}. This reduces the gain of both paths at high frequencies.

First we need the transfer function for the current mirror. To simplify the derivation, we lump several impedances to reduce the number of variables. The we use KCL to solve for the transfer functions

$$\text{para}(x,y) := \frac{x\cdot y}{x+y}$$

$$Z_1 = \text{para}\left(\frac{1}{s\cdot C_{gsN}}, \frac{1}{g_{mN}}\right) + R_1 + \text{para}\left(\frac{1}{s\cdot C_{\pi}}, \frac{1}{g_{mQ1}}\right)$$

$$Z_s = \text{para}\left(\frac{1}{s\cdot C_{\pi}\cdot N}, \frac{1}{g_{mQ1}}\right)$$

This section doesn't work

KCL @ V_i:

$$i_i = \frac{V_i}{Z_1} + (V_i - V_s)\cdot s\cdot C_{gsN}$$

KCL @ V_s:

$$(V_i - V_s)\cdot s\cdot C_{gsN} + g_{mN}\cdot(V_i - V_s) = \frac{V_s}{Z_s}$$

$$i_o = g_{mN}\cdot(V_i - V_s)$$

Solving for i_o/i_i yields

$$i_o = \frac{g_{mN}\cdot Z_1}{g_{mN}\cdot Z_s + 1}\cdot\frac{i_i}{\left[s\cdot\frac{C_{gsN}\cdot(Z_s + Z_1)}{g_{mN}\cdot Z_s + 1} + 1\right]}$$

We repeat the derivation for the M_3 gain stage

$$i_o = \frac{g_{mN}}{g_{mN}\cdot Z_s + 1}\cdot\frac{V_i}{\left(\frac{s\cdot C_{gsN}\cdot Z_s}{g_{mN}\cdot Z_s + 1} + 1\right)}$$

The overall open-loop gain transfer function becomes

$$A_{ol} = \frac{-g_{mN3}\cdot\text{para}(R_o, C_c)}{g_{mN3}\cdot Z_{s3} + 1}\cdot\frac{1}{\left[\frac{s\cdot C_{gsN3}\cdot(Z_{s3} + \text{para}(R_o, C_c))}{g_{mN3}\cdot Z_{s3} + 1} + 1\right]}\cdot\text{para}\left[\frac{1}{\frac{1}{g_{mMP3}}}, \frac{1}{s\cdot(C_{gsP3} + C_{gsP2} + C_{gsP1})}\right]\cdot\left[1 - \frac{g_{mN}\cdot Z_1}{g_{mN}\cdot Z_s + 1}\cdot\left[\right.\right.$$

A good approximation for the open-loop gain and the dominant pole are:

$$A_L = \frac{g_{mMN3}}{1 + g_{mMN3}\cdot\frac{1}{g_{mQ3}}}\cdot M\cdot R_o\cdot\left[1 - \frac{g_{mMN2}}{1 + g_{mMN2}\cdot\frac{1}{g_{mQ1}}}\cdot\left(\frac{1}{g_{mMN1}} + \frac{1}{g_{mQ1}} + R_1\right)\right]$$

$$p_1 = \frac{1}{R_o\cdot C_c}$$

Multiplying these two the open-loop unity gain bandwidth becomes

$$\omega_u = \left(\frac{g_{mMN1}}{1 + \frac{g_{mMN1}}{g_{mQ1}}} \right)^2 \cdot \frac{R_1}{C_C}$$

To insure good phase margin we need the unity gain bandwidth to be about 2 times lower than the lowest non-dominant pole under worst case conditions. From the transfer functions above it is difficult to tell which what the lowest non-dominant pole is, because of the pole-zero interactions. To simplify make following assumptions about the non-dominant poles:

$g_{mMN1} := \frac{2 \cdot I}{V_{DSsatN}}$ $g_{mMP3} := \frac{2 \cdot I}{M \cdot V_{DSsatN}}$ $g_{mQ1} := \frac{I}{V_T}$

$C_{gsMP3} := W_{Pbg} \cdot L_{Pbg} \cdot C_{OX}$ $C_{gsMP2} := W_P \cdot L_P \cdot C_{OX}$ $C_{gsMP1} := W_P \cdot L_P \cdot C_{OX}$ $C_{gsN} := W_N \cdot L_N \cdot C_{OX}$

$\omega_{p1} := \frac{g_{mMP3}}{(C_{gsMP3} + C_{gsMP2} + C_{gsMP1})}$ $\frac{\omega_{p1}}{2 \cdot \pi} = 0.13\,\text{GHz}$

$\omega_{p2} := \frac{1}{\left(\frac{1}{g_{mMN1}} + R_1 + \frac{1}{g_{mQ1}} \right) \cdot C_{gsN}}$ $\frac{\omega_{p2}}{2 \cdot \pi} = 0.01\,\text{GHz}$

Now we can solve for the required compensation capacitance

$$C_c := \left(\frac{g_{mMN1}}{1 + \frac{g_{mMN1}}{g_{mQ1}}} \right)^2 \cdot \frac{R_1 \cdot 2}{\min((\omega_{p1} \ \omega_{p2}))}$$

$C_c = 411.66\,\text{pF}$ This section doesn't work

Phase Margin and Compensation

Performance Measures

Performance Measures

$$\begin{aligned} \text{Area} := {} & 2 \cdot W_N \cdot (L_N + 2 \cdot L_{min}) + 2 \cdot W_P \cdot (L_P + 2 \cdot L_{min}) + 2 \cdot W_{Pcas} \cdot (L_{Pcas} + 2 \cdot L_{min}) \ldots \\ & + 2 \cdot W_{Pcasbias} \cdot (L_{Pcasbias} + 2 \cdot L_{min}) + 2 \cdot W_{Pbias} \cdot (L_{Pbias} + 2 \cdot L_{min}) \ldots \\ & + W_{Pbgcas} \cdot (L_{Pbgcas} + 2 \cdot L_{min}) + W_{Pbg} \cdot (L_{Pbg} + 2 \cdot L_{min}) \ldots \\ & + W_R \cdot (L_{R1} + L_{min}) + W_R \cdot (L_{R2} + L_{min}) + (N + 1) \cdot \text{Area}_{Q1} \ldots \\ & + W_{Pstart} \cdot (L_{Pstart} + 2 \cdot L_{min}) + W_{Nstart} \cdot (L_{Nstart} + 2 \cdot L_{min}) \end{aligned}$$

$\sqrt{\text{Area}} = 380.68\,\mu\text{m}$

$\sqrt{2 \cdot W_N \cdot (L_N + 2 \cdot L_{min})} = 352.44\,\mu\text{m}$ NMOS Area

$\sqrt{2 \cdot W_P \cdot (L_P + 2 \cdot L_{min}) + 2 \cdot W_{Pbias} \cdot (L_{Pbias} + 2 \cdot L_{min}) + W_{Pbg} \cdot (L_{Pbg} + 2 \cdot L_{min})} = 62.66\,\mu\text{m}$ PMOS Area

PMOS Cascode Area

$\sqrt{2 \cdot W_{Pcas} \cdot (L_{Pcas} + 2 \cdot L_{min}) + 2 \cdot W_{Pcasbias} \cdot (L_{Pcasbias} + 2 \cdot L_{min}) + W_{Pbgcas} \cdot (L_{Pbgcas} + 2 \cdot L_{min})} = 116.43\,\mu\text{m}$

$\sqrt{W_R \cdot (L_{R1} + L_{min}) + W_R \cdot (L_{R2} + L_{min})} = 44.91\,\mu\text{m}$ Resistor Area

$\sqrt{W_{Pstart} \cdot (L_{Pstart} + 2 \cdot L_{min}) + W_{Nstart} \cdot (L_{Nstart} + 2 \cdot L_{min})} = 15.12\,\mu\text{m}$ Start Up Circuit Area

Bipolar Area

$I_{VDD} := I \cdot \left(\frac{1}{3 \cdot S} + 1 + 1 + \frac{1}{M} + \frac{1}{M} + X \right)$ $I_{VDD} = 5.05 \times 10^3\,\mu\text{A}$

$\text{Power} := I_{VDD} \cdot V_{DDmax}$ $\text{Power} = 16.67\,\text{mW}$

$\text{Cost} := C_P \cdot \text{Power} + C_A \cdot \text{Area}$ $\text{Cost} = 1.96\,\text{cents}$

Ba naly

$$g_{mMN1} := \frac{2 \cdot I}{V_{DSsatN}} \quad g_{mMP1} := \frac{2 \cdot I}{V_{DSsatP}} \quad g_{mQ4} := \frac{I \cdot X}{V_T} \quad g_{mMP4} := \frac{2 \cdot I \cdot X}{V_{DSsatP}} \quad g_{mQ1} := \frac{I}{V_T}$$

$$v_{nQ4} := \sqrt{4 \cdot k \cdot Temp \cdot \frac{1}{2 \cdot g_{mQ4}}} \qquad v_{nMP4}(f) := \sqrt{4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot g_{mMP4}} + \frac{K_{fP}}{W_{Pbg} \cdot L_{Pbg} \cdot f}}$$

$$v_{nMN1}(f) := \sqrt{4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot g_{mMN1}} + \frac{K_{fN}}{W_N \cdot L_N \cdot f}} \qquad v_{nMP1}(f) := \sqrt{4 \cdot k \cdot Temp \cdot \frac{2}{3 \cdot g_{mMP1}} + \frac{K_{fP}}{W_P \cdot L_P \cdot f}}$$

$$v_{nR2} := \sqrt{4 \cdot k \cdot Temp \cdot R_2} \quad v_{nR1} := \sqrt{4 \cdot k \cdot Temp \cdot R_1} \qquad v_{nQ1} := \sqrt{4 \cdot k \cdot Temp \cdot \frac{1}{2 \cdot g_{mQ1}}}$$

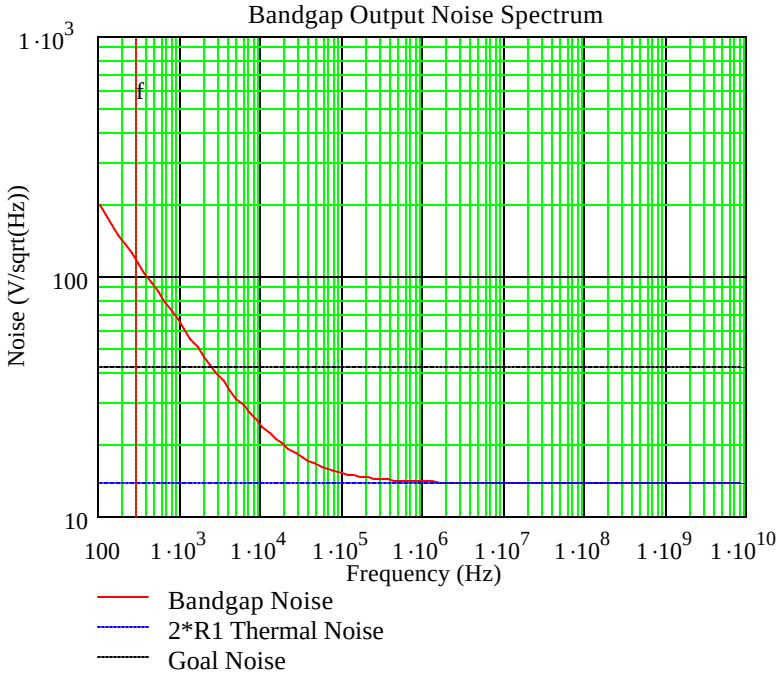
$$v_2(f) := \sqrt{\frac{2}{(g_{mMP1} \cdot R_1)^2} \cdot v_{nMN1}(f)^2 + \left[\frac{\left(1 + \frac{g_{mQ1}}{g_{mMN1}}\right)^2}{(R_1 \cdot g_{mQ1})^2} + \frac{\left(R_1 \cdot g_{mQ1} + \frac{g_{mQ1}}{g_{mMN1}} + 1\right)^2}{(R_1 \cdot g_{mQ1})^2} \right] \cdot v_{nMP1}(f)^2 \ldots + \frac{2 \cdot v_{nQ1}^2}{(g_{mMP1} \cdot R_1)^2} + \frac{v_{nR1}^2}{(g_{mMP1} \cdot R_1)^2}}$$

Now applying v_2^2 to find the output noise:

$$v_{bg}(f) := \sqrt{\left(v_2(f)^2 + v_{nMP4}(f)^2\right) \cdot g_{mMP4}^2 \cdot \left(R_2 + \frac{1}{g_{mQ4}}\right)^2 + v_{nR2}^2 + v_{nQ4}^2}$$

$f_{start} := 100Hz \qquad f_{stop} := 10GHz$

$$fval_i := f_{start} \cdot \left(\frac{f_{stop}}{f_{start}}\right)^{\frac{i-1}{num-1}}$$



$$\Delta R\_R := \sqrt{\frac{\Delta R\_R_{min}^2 \cdot W_{min}^2}{W_R^2}} \qquad \Delta R\_R = 4\%$$

Resistor Variation ,where

$$\Delta V_{thP} := \sqrt{\Delta V_{thPLmin}^2 \cdot \frac{L_{min}^2}{2}} \qquad \Delta V_{thP} = 3.89\,mV$$

3s PMOS Threshold Variation,

Ba $\sqrt{\quad L_P^2}$ ... where

$$\Delta V_{thN} := \sqrt{\Delta V_{thNLmin}^2 \cdot \frac{L_{min}^2}{L_N^2}} \qquad \Delta V_{thN} = 5.55\,mV$$

3s PMOS Threshold Variation, where

$$\Delta I\_I_{mir} := \sqrt{\Delta V_{thP}^2 \cdot \left(\frac{2}{V_{DSsatP}}\right)^2 + \sigma_{\Delta W}^2 \cdot \left(\frac{\mu_P \cdot C_{OX} \cdot V_{DSsatP}^2}{2 \cdot I \cdot L_P}\right)^2 + \frac{\sigma_{\Delta L}^2}{L_P^2}} \qquad \Delta I\_I_{mir} = 4.1\,\%$$

Current Mirror Mismatch

$$Area_{Q1min} := (1\mu m)^2 \qquad \Delta Is\_Is_{Areamin} := 5\%$$

$$\Delta Is\_Is := \sqrt{\Delta Is\_Is_{Areamin}^2 \cdot \frac{Area_{Q1min}}{Area_{Q1}}} \qquad \Delta Is\_Is = 0.48\,\%$$

Bipolar Transistor Reverse Satu

$$\Delta V_{bgmismatch} := \sqrt{V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \left[\frac{\Delta R\_R^2}{\frac{R_2}{R_1}} + \Delta I\_I_{mir}^2 \cdot \left[\left(1 + \frac{\frac{V_{DSsat}}{2 \cdot V_T} + 1}{\ln(N)}\right)^2 + \frac{1}{X}\right] \ldots + \left[\frac{\Delta Is\_Is^2}{N} + \left[\left(\frac{\sigma_{\Delta L}}{L_N}\right)^2 + \left(\frac{\sigma_{\Delta W}}{W_N}\right)^2\right] \cdot \left(\frac{V_{DSsatN}}{2 \cdot V_T}\right)^2 + \frac{\Delta V_{thN}^2}{V_T^2}\right] \cdot \frac{1}{\ln(N)^2}\right]}$$

$$\frac{\Delta V_{bgmismatch}}{V_{bg}} = 38.64\,\%$$

The bandgap variance due to mismatch

$$\frac{\sqrt{V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \frac{\Delta R\_R^2}{\left(\frac{R_2}{R_1}\right)}}}{V_{bg}} = 0.53\,\%$$

Resistor Mismatch

$$\frac{\sqrt{V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \left[\left(\frac{\Delta Is\_Is^2}{N}\right) \cdot \frac{1}{\ln(N)^2}\right]}}{V_{bg}} = 0.03\,\%$$

Bipolar Mismatch

$$\frac{\sqrt{V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \left[\left[\left[\left(\frac{\sigma_{\Delta L}}{L_N}\right)^2 + \left(\frac{\sigma_{\Delta W}}{W_N}\right)^2\right] \cdot \left(\frac{V_{DSsatN}}{2 \cdot V_T}\right)^2 + \frac{\Delta V_{thN}^2}{V_T^2}\right] \cdot \frac{1}{\ln(N)^2}\right]}}{V_{bg}} = 4.1\,\%$$

NMOS Mismatch

$$\frac{\sqrt{V_T^2 \cdot \left(\frac{R_2}{R_1} \cdot X \cdot \ln(N) + 1\right)^2 \cdot \Delta I\_I_{mir}^2 \cdot \left[\left(1 + \frac{\frac{V_{DSsat}}{2 \cdot V_T} + 1}{\ln(N)}\right)^2 + \frac{1}{X}\right]}}{V_{bg}} = 38.41\,\%$$

PMOS Mismatch

$C_{je} := 14fF \qquad \tau_F := 10pS$

$C_\pi := C_{je} + g_{mQ1} \cdot \tau_F \qquad C_{\pi N} := C_{je} \cdot N + g_{mQ1} \cdot \tau_F \qquad g_{mQ3} := \frac{I}{M \cdot V_T} \qquad C_{\pi 3} := \frac{C_{je}}{M} + g_{mQ3} \cdot \tau_F$

g_{mMI}

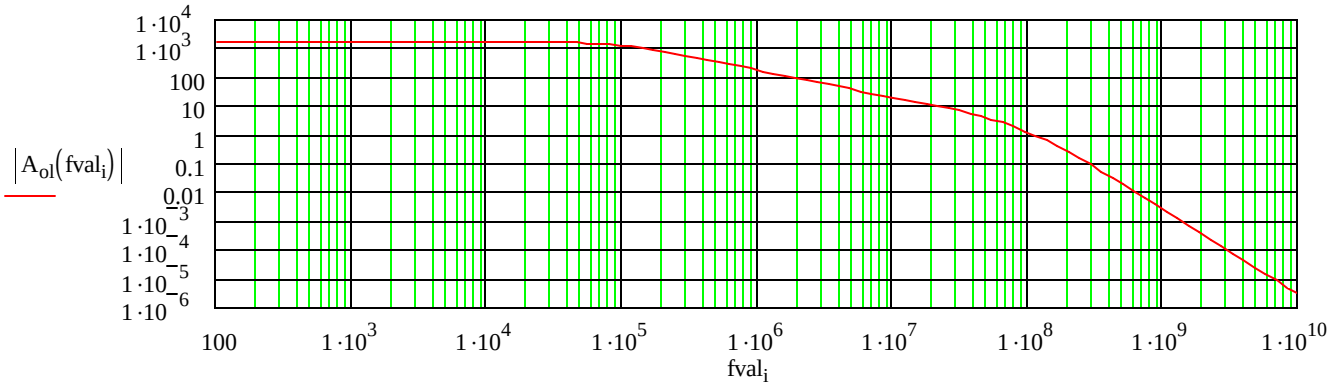
$Z_1(s) := para\left(\frac{1}{s \cdot C_{gsN}}, \frac{1}{g_{mMN1}}\right) + R_1 + para\left(\frac{1}{s \cdot C_\pi}, \frac{1}{g_{mQ1}}\right)$

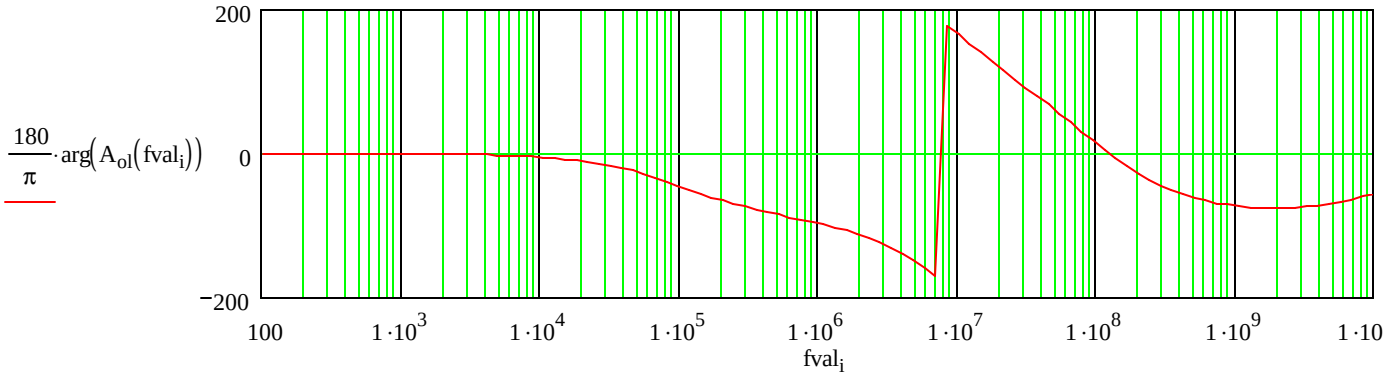
$$Z_s(s) := \text{para}\left(\frac{1}{s \cdot C_{\pi N}}, \frac{1}{g_{mQ1}}\right)$$

$$Z_{s3}(s) := \text{para}\left(\frac{1}{s \cdot C_{\pi 3}}, \frac{1}{g_{mQ3}}\right)$$

$$C_{gsN3} := W_{Nbias} \cdot L_{Nbias} \cdot C_{OX}$$

$$A_{ol}(f) := \left| s \leftarrow \sqrt{-1} \cdot 2 \cdot \pi \cdot f \right.$$
$$\left. \frac{-g_{mMN3} \cdot \text{para}\left(R_o, \frac{1}{s \cdot C_c}\right)}{g_{mMN3} \cdot Z_{s3}(s) + 1} \cdot \frac{1}{\left[\frac{s \cdot C_{gsN3} \cdot \left(Z_{s3}(s) + \text{para}\left(R_o, \frac{1}{s \cdot C_c}\right)\right)}{g_{mMN3} \cdot Z_{s3}(s) + 1} + 1\right]} \cdot \text{para}\left[\frac{1}{g_{mMP3}}, \frac{1}{s \cdot (C_{gsMP3} + C_{gsMP2} + C_{gsMP}}\right.$$





Performance Measures

Outputs

Outputs: Device Sizes for CMOS Bandgap with Low Sensitivity to Rout.

Bias Generator	PTAT Generator	Bandgap Generator	Start-Up Circuit
$L_{Pcasbias} = 0.5\,\mu m$	$L_{Pcas} = 0.5\,\mu m$	$R_2 = 0.33\,k\Omega$	$W_{Pstart} = 74.78\,\mu m$
$W_{Pcasbias} = 16.88\,\mu m$	$W_{Pcas} = 3 \times 10^3\,\mu m$	$W_{Pbg} = 373.9\,\mu m$	$L_{Pstart} = 2\,\mu m$
$L_{N...} = 2\,\mu m$	$L_{N...} = 2\,\mu m$	$L_{P...} = 2\,\mu m$	$W_{N...} = 1\,\mu m$

$L_{Pbias} = 2\,\mu m$

$W_{Pbias} = 93.47\,\mu m$

$W_{Nbias} = 5.18 \times 10^{3}\,\mu m$

$L_{Nbias} = 2\,\mu m$

$L_N = 2\,\mu m$

$W_N = 20.7\,mm$

$W_P = 373.9\,\mu m$

$L_P = 2\,\mu m$

$R_1 = 39.36\,\Omega$

$W_R = 101.62\,\mu m$

$L_{R1} = 2\,\mu m$

$L_{Pbg} = 2\,\mu m$

$W_{Pbgcas} = 3 \times 10^{3}\,\mu m$

$L_{Pbgcas} = 0.5\,\mu m$

$W_R = 101.62\,\mu m$

$L_{R2} = 16.85\,\mu m$

$W_{Nstart} = 1\,\mu m$

$L_{Nstart} = 3.13\,\mu m$

The following "variables" are redefined to "figure variables" so that a different font could be used.

$L_{Pcasbias} := L_{Pcasbias}$

$W_{Pcasbias} := W_{Pcasbias}$

$L_{Pbias} := L_{Pbias}$

$W_{Pbias} := W_{Pbias}$

$W_{Nbias} := W_{Nbias}$

$L_{Nbias} := L_{Nbias}$

$L_{Pcas} := L_{Pcas}$

$W_{Pcas} := W_{Pcas}$

$L_N := L_N$

$W_N := W_N$

$L_P := L_P$

$W_P := W_P$

$R_1 := R_1$

$W_R := W_R$

$R_2 := R_2$

$W_{Pbg} := W_{Pbg}$

$L_{Pbg} := L_{Pbg}$

$W_{Pbgcas} := W_{Pbgcas}$

$L_{Pbgcas} := L_{Pbgcas}$

$L_{R2} := L_{R2}$

$L_{R1} := L_{R1}$

$W_{Pstart} := W_{Pstart}$

$L_{Pstart} := L_{Pstart}$

$W_{Nstart} := W_{Nstart}$

$L_{Nstart} := L_{Nstart}$

$M := M$

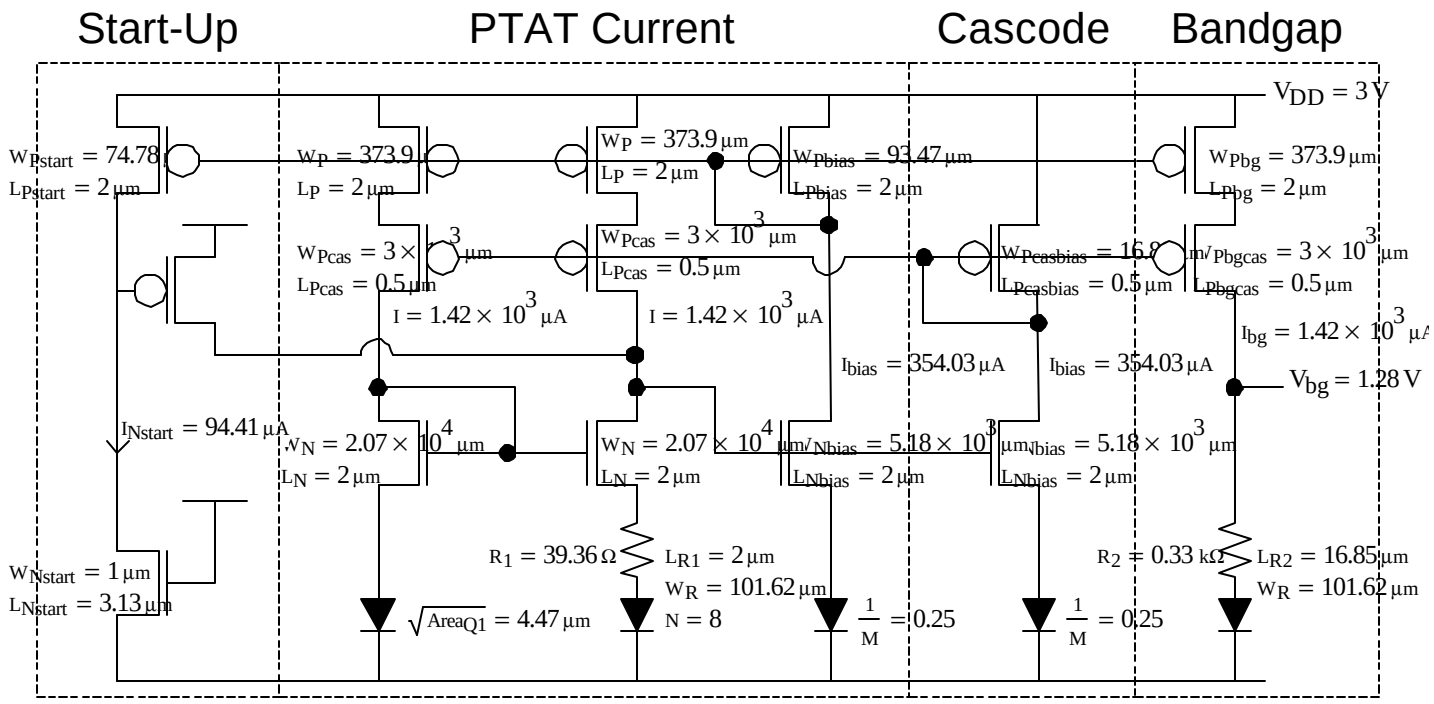
$I := I$

$I_{bias} := I_{bias}$

$I_{bg} := I_{bg}$

$I_{Nstart} := I_{Nstart}$

Outputs



Power = 16.67 mW $\quad \sqrt{Area} = 380.68\,\mu m$ $\quad$ Cost = 1.96 cents $\quad v_n = 41.44 \frac{nV}{\sqrt{Hz}}$ $\quad \frac{\Delta V_{bgmismatch}}{V_{bg}} = 38.64\%$ $V_{DDbgmin}$

$I_{VDD} = 5.05\,mA$

Fig. 1: CMOS bandgap and start-up circuit with device sizes

The following stages use the PTAT current from the bandgap generator.

$W_{PTAT} := W_P$

$I_{PTAT} := I$

$L_{PTAT} := L_P$

Noise and variance of the resistor divided bandgap voltage

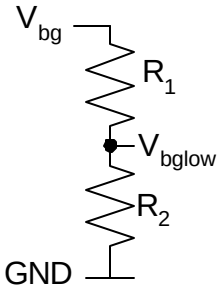


Fig. 1: Bandgap Voltage w/ Resistor Divider

The bandgap voltage is often passed to another circuit, which requires a reduced value of the bandgap voltage, where the reduction comes from a resistor divider. This section analyzes the noise and variance of the resistor divider. For example purposes we assume the reduced

$$V_{bglow} = V_{bg}\cdot\frac{R_2}{R_1 + R_2}$$

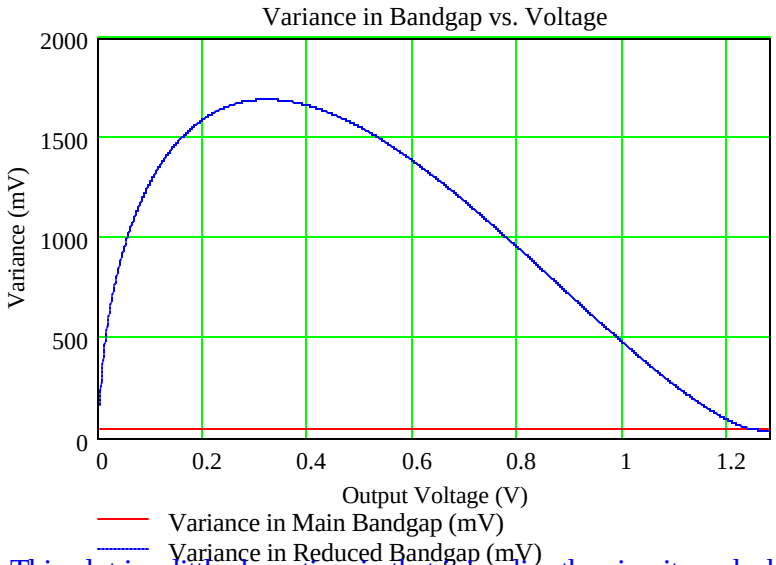
Variance of reduced bandgap voltage:

$$R_1 = R \qquad R_2 = R2\_R1\cdot R\left(1 + \frac{\sigma_{\Delta R}}{R\cdot\sqrt{R2\_R1}}\right) \qquad V_{bg} = V_{bg} + \sigma_{\Delta Vbg}$$

$$\sigma_{\Delta Vbglow} = V_{bg}\cdot\frac{R_2}{R_1 + R_2}\cdot\sqrt{\frac{\sigma_{\Delta R\_R}^{2}}{\left(\frac{R_2 + R_1}{R_1}\right)^2\cdot\frac{R_2}{R_1}} + \left(\frac{\sigma_{\Delta Vbg}}{V_{bg}}\right)^2}$$

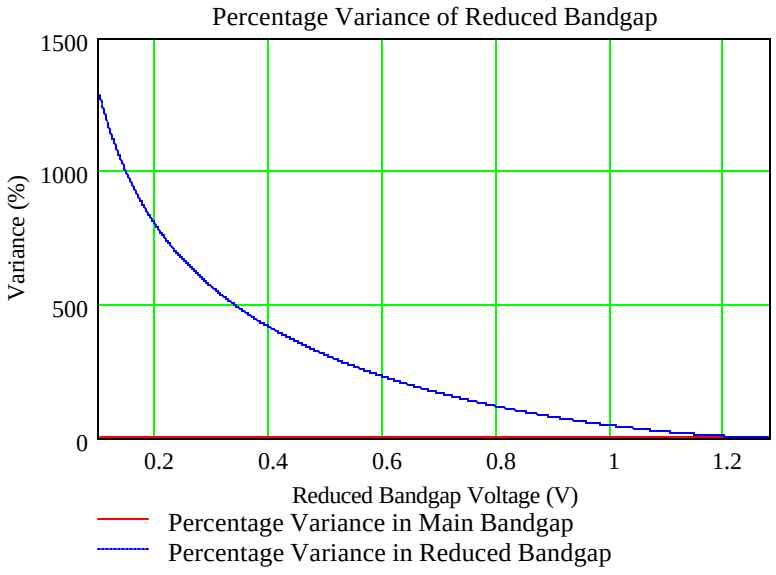
If we plot the variance of the output voltage vs. V_{bglow}:

$$\sigma_{\Delta Vbglow} = V_{bglow}\cdot\sqrt{\frac{\sigma_{\Delta R\_R}^{2}}{\left(\frac{V_{bg}}{V_{bg} - V_{bglow}}\right)^2\cdot\frac{V_{bglow}}{V_{bg} - V_{bglow}}} + \sigma_{\Delta Vbg\_Vbg}^{2}}$$



This plot is a little deceptive, in that it implies the circuit works better for reduced output voltages. In reality, the percentage variance in output voltage is greater as can be seen from the following plot.

Bandg



led down bandgap voltage as close to the original bandgap voltage as possible, limited by headroom constraints. We also notice for reductions up to 1/2 of the bandgap voltage, the variance of the divided bandgap voltage is about the same as the main bandgap. This is partly because of the good matching of resistors used for the plot.

Noise of the reduced bandgap voltage

A note when sizing the components for noise, it is important to size them for noise at the highest operating temperature. This is where the noise is typically the largest.

$$\sigma_{Vnbglow} = \left(\sigma_{Vnbg}^{2} + \sigma_{VnR1}^{2}\right)\cdot\left(\frac{R_2}{R_1 + R_2}\right)^{2} + \sigma_{VnR2}^{2}\cdot\left(\frac{R_1}{R_1 + R_2}\right)^{2}$$

Making the following substitutions and simplifying

$$\sigma_{VnR1}^{2} = 4\cdot k\cdot T\cdot R_1 \qquad \sigma_{VnR2}^{2} = 4\cdot k\cdot T\cdot R_2 \qquad R_2 = \frac{V_{bglow}}{V_{bg}}\cdot R_{tot} \qquad R_1 = \left(1 - \frac{V_{bglow}}{V_{bg}}\right)\cdot R_{tot}$$

Yields the following result

$$\sigma_{Vnbglow}^{2} = \sigma_{Vnbg}^{2}\cdot\left(\frac{V_{bglow}}{V_{bg}}\right)^{2} + 4\cdot k\cdot T\cdot R_{tot}\cdot\left(1 - \frac{V_{bglow}}{V_{bg}}\right)\cdot\frac{V_{bglow}}{V_{bg}}$$

Or normalized this gives:

$$\frac{\sigma_{Vnbglow}^{2}}{V_{bglow}^{2}} = \frac{\sigma_{Vnbg}^{2} + 4\cdot k\cdot T\cdot R_{tot}\cdot\left(\frac{V_{bg}}{V_{bglow}} - 1\right)}{V_{bg}^{2}}$$

If we look at noise on a percentage basis using **EQUAL** current in the resistor divider as the bandgap, using the following noise estimate for the bandgap circuit, we see the resistor divider contributes 10% to the total noise and the bandgap contributes 90%. Thus we size Rtot for about 20% of the noise budget.

$\sigma_{nVbg}^{2} = 4\cdot k\cdot Temp\cdot K_{ptat}^{2}\cdot\frac{2\cdot V_T}{I_{dd}}$ bandgap quick noise approximation (sized for current)

$R_{tot} = \frac{V_{bg}}{I_{dd}}$ $V_{bglow} := \frac{V_{bg}}{2}$ R_{tot} sized for current

$$\frac{K_{ptat}^{2}\cdot V_T}{\left(V_{bg}\right)^{2}} = 86.52\,\% \qquad \frac{V_{bg}\cdot\left(\frac{V_{bg}}{V_{bglow}} - 1\right)}{\left(V_{bg}\right)^{2}} = 13.48\,\%$$

Bandg $K_{ptat}^2 \cdot V_T + V_{bg}\left(\frac{V_{bg}}{V_{bglow}} - 1\right)$ $K_{ptat}^2 \cdot V_T + V_{bg}\left(\frac{V_{bg}}{V_{bglow}} - 1\right)$

From this equation we see that we can size the resistor to give us the desired noise voltage.

$$R_{tot} = \frac{20\% \cdot \sigma_{Vbglown}^2}{4 \cdot k \cdot Temp} \cdot \left(\frac{V_{bg}}{V_{bglow}}\right)^2 \cdot \left(\frac{V_{bglow}}{V_{bg} - V_{bglow}}\right)$$

Noise & Variance of Res.Divider

Voltage to Current Converters

Op-Amp Based Bandgap Voltage to Current Converter

An important concept to consider, when designing op-amp based bandgap buffers is where it's bias current will come from. The two most popular options are constant g_m circuits, MOS and bipolar, but there are many other possibilities including constant slewing, etc.. In the bipolar case, we can simply use the PTAT current available from the bandgap circuit. In the MOS case, a separate constant-gm current generator will have to be created. This will require more current in the IC, but is acceptable if the current will be reused, or if it helps to save current, by reducing process variations in a MOS op-amp of the voltage-to-current converter.

Other important effects to consider, when designing operational amplifier circuits are:

a) Stability: especially in the presence of extra capacitance from bonding pads, board traces, and probe capacitances.

b) Sensitivity of nodes to high frequency disturbances. Op-amps do little good at suppressing nonidealities beyond their unity gain bandwidth.

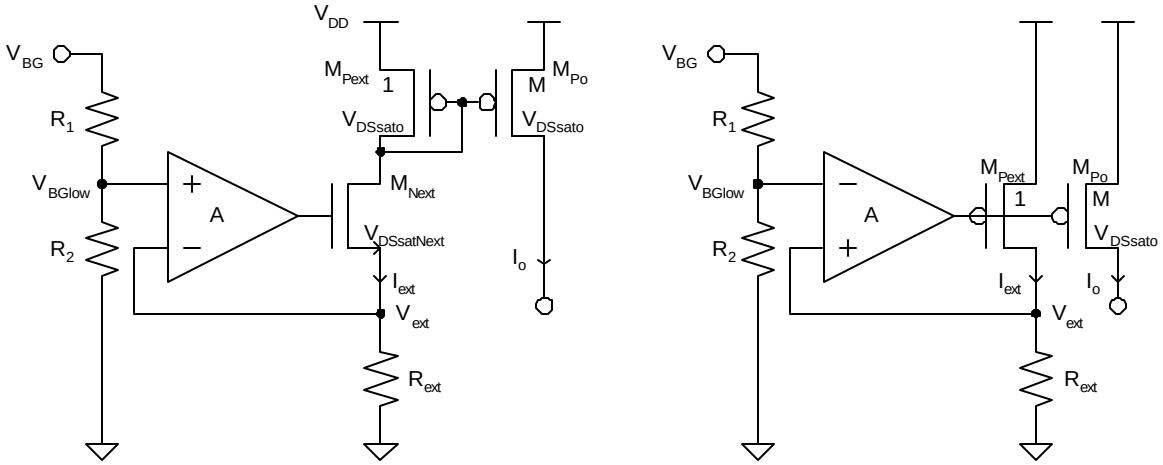


Fig. 1: Bandgap Current Generator Circuits

In general the bandgap will be turned into a current, where it will be mirrored of to another circuit. We can assume two scenarios for where the current will be used. In scenario 1, V_{DSsat} will be made small to maximize headroom, in this case V_{DSsat} will be given.

In the second scenario V_{DSsat} will be maximized to minimize noise. In this scenario, either V_{DSsat} will be given again, or the voltage-to-current converter will be designed to maximum the load current mirror's V_{DSsat}. The following design options will be explored for current converter.

Option #1. Mirror Bandgap current from bandgap's emitter follower

Option #2. Op-amp based voltage to current converter with NMOS Follower

2a. Single-stage NMOS input op-amp

2b. Single-stage PMOS input op-amp

2c. Two-stage NMOS input op-amp

2d. Two-stage PMOS input op-amp

Option #3: Op-amp based voltage to current converter with PMOS Mirror

3a. Single-stage NMOS input op-amp

3b. Single-stage PMOS input op-amp

3c. Two-stage NMOS input op-amp

3d. Two-stage PMOS input op-amp

For each option, the following variables will be found and summarized in a table:

1. Maximum load V_{DSsat}.
2. Minimum supply voltage for a given load V_{DSsat}.
3. Noise Current Assuming a Folded Cascode Operational Amplifer for two-stage (1/f noise must be considered)
4. Variance in Output Voltage

Output voltage noise

In the following derivations the output current noise from option #2 and option #3 are identical. The noise at the gate of the output transistor is

KCL @ Vext:

$$g_{mNo}\cdot\left[v_{nNext} + A\cdot\left(v_{noa} + v_{bglow} - v_{ext}\right)\right] = \frac{v_{ext} + v_{nRext}}{R_{ext}}$$

$$i_{ext} = g_{mNo}\cdot\left[v_{nNext} + A\cdot\left(v_{noa} + v_{bglow} - v_{ext}\right)\right]$$

$$i_o = M\cdot i_{ext} + \left(v_{nPext} + v_{nPo}\right)\cdot g_{mo}$$

Solving for io:

$$i_o = \frac{\left(M\cdot g_{mNo}\cdot A\cdot v_{noa} + M\cdot g_{mNo}\cdot A\cdot v_{bglow} + M\cdot g_{mNo}\cdot A\cdot v_{nRext} + g_{mo}\cdot v_{nPext}\cdot g_{mNo}\cdot A\cdot R_{ext} + g_{mo}\cdot v_{nPo}\cdot g_{mNo}\cdot A\cdot R_{ext}\right)}{\left(g_{mNo}\cdot A\cdot R_{ext}\right)}$$

Assuming the operational amplifier gain is large:

$$i_{on}^2 = \left(\frac{M}{R_{ext}}\right)^2\cdot\left(v_{noa}^2 + v_{bglow}^2 + v_{nRext}^2\right) + g_{mPo}^2\cdot\left(v_{nPext}^2 + v_{nPo}^2\right)$$

We can also that the output current noise is more a function of the ratio of the bandgap noise to the bandgap voltage than the bandgap noise itself. Thus it is desirable to keep Vbglow as large as possible. From this equation we five sources of noise: The bandgap, the opamp, the resistor, and the two current mirror transistors. The resistor itselft contributes a negligible amount of noise. The output current mirror contributes a given amount of noise, which is fixed by the input constraints of I_o and V_{DSsat}. This leaves budgeting only for the bandgap, op-amp and current mirror. Two quick approximations for the op-amp and bandgap are given below:

$$\sigma_{Vnoa}^2 = 2\cdot 4\cdot k\cdot Temp\cdot\frac{2}{3\cdot g_{mi}} = 2\cdot 4\cdot k\cdot Temp\cdot\frac{2\cdot V_{DSsatin}\cdot NF}{3\cdot I_{tail}}$$ MOS Op-amp quick approximation

$$\sigma_{Vnoa}^2 = 2\cdot 4\cdot k\cdot Temp\cdot\frac{V_T}{I_{tail}}$$ Bipolar Op-amp quick approximation

$$\sigma_{Vbglow}^2 = \frac{K_{Nbg}}{I_{bg}}$$ bandgap quick approximation

$$\sigma_{VnRext}^2 = 4\cdot k\cdot Temp\cdot R_{ext}$$ Noise of External Resistor

$$\sigma_{VnPext}^2 = 4\cdot k\cdot Temp\cdot\frac{2}{3\cdot g_{mPext}}$$

$$\sigma_{VnPo}^2 = 4\cdot k\cdot Temp\cdot\frac{2}{3\cdot g_{mPo}}$$

Making the following variable substitutions

Making the following variable substitutions

$$R_{ext} = \frac{V_{bglow}}{I_{ext}} \qquad M = \frac{I_o}{I_{ext}} \qquad g_{mPo} := \frac{2 \cdot I_o}{V_{DSsato}} \qquad g_{mPext} = \frac{2 \cdot I_{ext}}{V_{DSsato}}$$

$$\sigma_{Ion}^{\ 2} = 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \left[\frac{4 \cdot V_{DSsatin} \cdot NF}{3 \cdot I_{tail}} + \frac{K_{Nbg}}{4 \cdot k \cdot Temp \cdot I_{bg}} + \frac{V_{bglow}}{I_{ext}} \cdot \left(1 + \frac{4 \cdot V_{bglow}}{3 \cdot V_{DSsato}} \right) + \frac{(2 \cdot V_{bglow})^2}{3 \cdot I_o \cdot V_{DSsato}} \right]$$

For the same current the bandgap is 100(MOS Input)-800(Bipolar Input) times noisier than the op-amp, so little noise budget should go to the op-amp. For the same current we also see the bandgap is around 7 times noisier than the current mirror. For optimization of the total current we represent the current noise in the following form:

$$\sigma_{Ion}^{\ 2} - 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \frac{(2 \cdot V_{bglow})^2}{3 \cdot I_o \cdot V_{DSsato}} = \frac{X_1}{I_{tail}} + \frac{X_2}{I_{ext}} + \frac{X_3}{I_{bg}}$$

$$X_1 = 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \frac{4 \cdot V_{DSsatin} \cdot NF}{3}$$

$$X_2 = 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot V_{bglow} \cdot \left(1 + \frac{4 \cdot V_{bglow}}{3 \cdot V_{DSsato}} \right)$$

$$X_3 = 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \frac{K_{Nbg}}{4 \cdot k \cdot Temp}$$

The total current is expressed as

$$I_{tot} = I_{bg} + I_{tail} + I_{ext}$$

The optimal values for current as derived earlier in the report are:

$$I_{totopt} = \frac{\left(\sqrt{X_1} + \sqrt{X_2} + \sqrt{X_3} \right)^2}{\sigma_{Ion}^{\ 2} - 4 \cdot k \cdot Temp \cdot \frac{2 \cdot 2 \cdot I_o}{3 \cdot V_{DSsato}}}$$

$$I_{bg} = \sqrt{\frac{I_{totopt}}{\sigma_{Ion}^{\ 2} - 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \frac{(2 \cdot V_{bglow})^2}{3 \cdot I_o \cdot V_{DSsato}}} \cdot X_1}$$

$$I_{tail} = \sqrt{\frac{I_{totopt}}{\sigma_{Ion}^{\ 2} - 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \frac{(2 \cdot V_{bglow})^2}{3 \cdot I_o \cdot V_{DSsato}}} \cdot X_2}$$

$$I_{ext} = \sqrt{\frac{I_{totopt}}{\sigma_{Ion}^{\ 2} - 4 \cdot k \cdot Temp \cdot \left(\frac{I_o}{V_{bglow}} \right)^2 \cdot \frac{(2 \cdot V_{bglow})^2}{3 \cdot I_o \cdot V_{DSsato}}} \cdot X_3}$$

$$R_{ext} = \frac{V_{bglow}}{I_{ext}}$$

Since R is external it must be chosen from a set of standard component values. We will choose the closest one: The difference in cost between a 1% resistor and 5% resistor is 0.015cents, and is negligible, so it is routine to use the 1% components. 1% Resistors are sorted after fabrication, so the distribution of values are usually not gaussian, but rather uniform over +/-1%. If a component is chosen to the closest standard value, the maximum potential error will be 2*1%=2% with an uneven distribution of 0% on one side an 2% on the other side. Thus the circuit can be systematically tuned to account recenter the output current to save 1% in variation.

$$R_{ext} = r_{find}(R_{ext})$$

Now the value for M, the current mirror ratio, can be found:

$$M = \frac{I_o \cdot R_{ext}}{V_{bglow}}$$

A possible method sizing the voltage-to-current converter is to do whatever is convenient for stability. Also note the op-amp with MOS inputs will contribute a significant amount of variance in the output current. This should also be considered in the sizing. Also these noise estimates only consider thermal noise. For low frequencies the equations should be redesigned for 1/f noise.

Variance of Op-Amp Based VtoI Converter

Now lets calculate the noise and variance of the output current. To do this we model first model the amplifier as an ideal op-amp with an input offset and input noise source. If this is true, then the noise from the NMOS follower doesn't matter. The output current is then

$$I_{out} = \frac{V_{bglow}}{R_{ext}} \cdot M$$

To find the variance in the output current, we make the following substitutions:

$$V_{bglow} = V_{bglow} \cdot \left(1 + \frac{\sigma_{Vbglow}}{V_{bglow}} \right) + \sigma_{\Delta Vopamp} \qquad R_{ext} = R_{ext} \cdot \left(1 + \sigma_{\Delta R\_Rext} \right)$$

Here we are assuming the resistor to be used is an external resistor with a tolerance of 1%. External resistors are commonly used to set the bias current for two reasons. First it gives the user flexibility in setting the current. Second, it reduces the variation in the current. On chip resistors can vary up to 30%, while external resistors can be purchased with variances down to 0.1%.

$$\sigma_{\Delta Io\_Io} = \frac{\sigma_{\Delta Vbglow}}{V_{bglow}} + \frac{\sigma_{\Delta Vopamp}}{V_{bglow}} + \sigma_{\Delta R\_Rext}$$

For design the variance in I_o must be budgeted among the bandgap, the op-amp and the external resistor

$$\sigma_{\Delta Vopamp} = \frac{K_{misoa}}{Area_{oa}}$$

Voltage to Current Converters

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