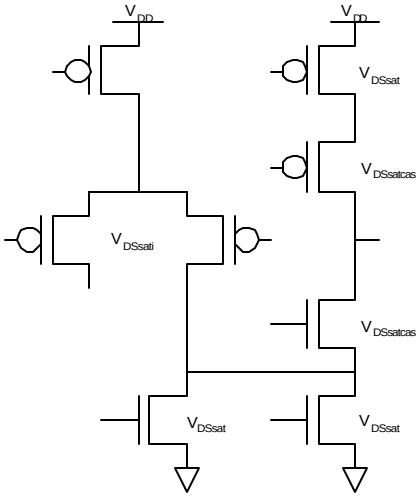
Optimal V_{DSsat} for Folded Cascode Amplifier



useful functions and identities
Units
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Introduction

This routine calculates the optimal V_{DSsat} of the bias current output transistors (i.e. not the cascode) of a folded cascode amplifier. Folded cascodes tend to be noisier, and have worse offsets, because they require an extra current mirror. They have one advantage, that the input common-mode is decoupled from the output swing. This makes them useful for non-inverting amplifier configurations. The optimal V_{DSsat}, is sized for maximum SNR. A small V_{DSsat} make the signal swing larger, but a large V_{DSsat} make the input referred noise of the current source smaller. The optimum is somewhere in between as calculated below. Coincidentally it is very close to the ubiquitous V_{DSsat} approximation of $V_{DD}/10$. It is also insensitive to process variations, as all optimized parameters values are.

Inputs

$V_{DD} := 2.7V$ Supply Voltage

$V_{DSsatcas} := 0.15V$ Cascode V_{DSsat}

$SNR := 82$ Desired Signal to Noise Ratio

$V_{DSsati} := 0.2V$ V_{DSsat} of Input Devices

$f_s := 2MHz$ Sampling Frequency

$Temp := 300K$ Temperature

$num := 100$ Number of Points

SNR Calculation

The signal swing of a folded cascode is reduced for increasing V_{DSsat} of the current sources.

$$V_{swing} = V_{DD} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSsat}$$

For class A amplifiers, used in switched capacitor applications, the current is sized for slewing, where the slew rate is proportional to load capacitance. The load capacitance is proportional to sampling capacitance, which is in turn sized for integrated noise. In load VDSsat optimization example, minimizing load capacitance requirement is equivalent to minimizing current, as terms such as SNR, settling time, etc. show up as scaling factors.

The input referred noise of a unity-gain configuration amplifier is

$$v_{nin}^2 = 4 \cdot k \cdot Temp \cdot \frac{\gamma}{g_{mi}} + 3 \cdot 4 \cdot k \cdot Temp \cdot \frac{\gamma}{g_m}$$

The factor of three comes from the three load transistors: two NMOS at the bottom of figure 1, and one PMOS at the top of figure one. Substituting an expression for the gms, the input referred noise becomes:

$$g_{mi} = \frac{2 \cdot I}{V_{DSsati}} \qquad g_m = \frac{2 \cdot I}{V_{DSsat}}$$

$$v_{nin}^2 = 2 \cdot 4 \cdot k \cdot Temp \cdot \frac{\gamma}{g_{mi}} \cdot \left(1 + 3 \cdot \frac{V_{DSsat}}{V_{DSsati}} \right)$$

The bandwidth of a unity-gain connected amplifier is

$$\omega_u = \frac{g_{mi}}{C}$$

For switched capacitor circuits, the noise folds down from the entire amplifier bandwidth, resulting in an integrated noise at the output of

$$v_{outint} = \int_0^{\infty} \frac{v_{nin}^2}{1 + \left(\frac{f}{f_u} \right)^2} df = 2 \cdot k \cdot Temp \cdot \frac{\gamma}{g_{mi}} \cdot \left(1 + 3 \cdot \frac{V_{DSsat}}{V_{DSsati}} \right) \cdot \frac{g_{mi}}{C}$$

Dividing the rms signal swing by the integrated noise we get the SNR

$$SNR = 10 \cdot \log \left[\frac{\frac{\left(V_{DD} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSsat} \right)^2}{8}}{2 \cdot k \cdot Temp \cdot \frac{\gamma}{g_{mi}} \cdot \left(1 + 3 \cdot \frac{V_{DSsat}}{V_{DSsati}} \right) \cdot \frac{g_{mi}}{C}} \right]$$

Solving for the required capacitance we get:

$$C = \frac{16 \cdot k \cdot Temp \cdot \gamma \cdot \left(1 + 3 \cdot \frac{V_{DSsat}}{V_{DSsati}} \right)}{\left(V_{DD} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSsat} \right)^2} \cdot 10^{\frac{SNR}{10}}$$

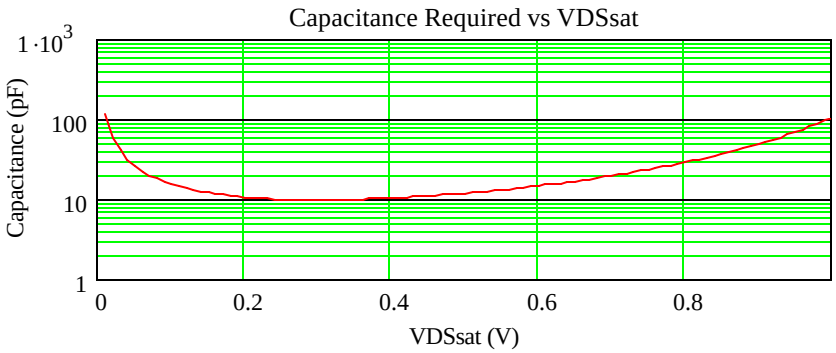
V_{DSsat} Optimization

Here V_{DSsat} is swept to show the capacitance curve is amenable to optimizing V_{DSsat}.

$i := 1..num$ Index Vector

$V_{DSsat_i} := \frac{i}{num} \cdot 1V$ V_{DSsat} vector

$$C_i := \frac{16 \cdot k \cdot Temp}{\left(V_{DD} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSsat_i}\right)^2} \cdot \left(1 + 3 \cdot \frac{V_{DSsati}}{V_{DSsat_i}}\right) \cdot 10^{\frac{SNR}{10}}$$ Load Capacitance



Take derivative of capacitance with respect to V_{DSsat} to find the optimal V_{DSsat} to minimize capacitance, and thus power dissipation.

$$\frac{d}{dV_{DSsat}} \frac{1 + 3 \cdot \frac{V_{DSsati}}{V_{DSsat}}}{\left(V_{DD} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSsat}\right)^2}$$

$$V_{DSsat}^{\ 2} + \frac{9}{2} \cdot V_{DSsati} \cdot V_{DSsat} + \frac{-3}{4} \cdot V_{DSsati} \cdot \left(V_{DD} - 2 \cdot V_{DSsatcas}\right) = 0$$

The optimal V_{DSsat} is then given by the following expression. Note that it is independent of SNR, current, settling time. It turns out to be a weak function of V_{DSsati} of the input pair, and a strong function of V_{DD}.

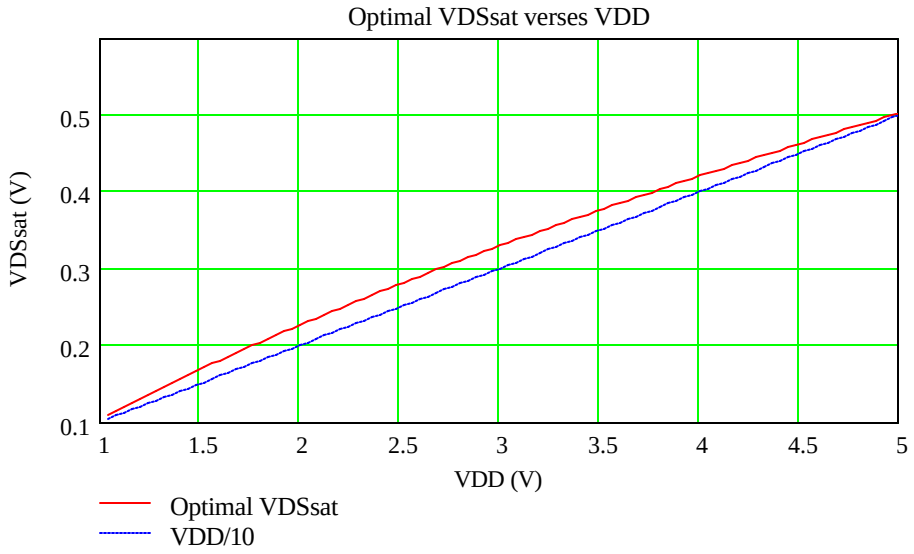
$$V_{DSopt}(V_{DD}) := \frac{-9}{4} \cdot V_{DSsati} \cdot \left[1 - \sqrt{1 + \frac{4 \cdot \left(V_{DD} - 2 \cdot V_{DSsatcas}\right)}{27 \cdot V_{DSsati}}}\right]$$ $V_{DSopt}(V_{DD}) = 0.3\,V$

If V_{DD} is swept, we can see how the optimal V_{DSsat} changes verses V_{DD}.

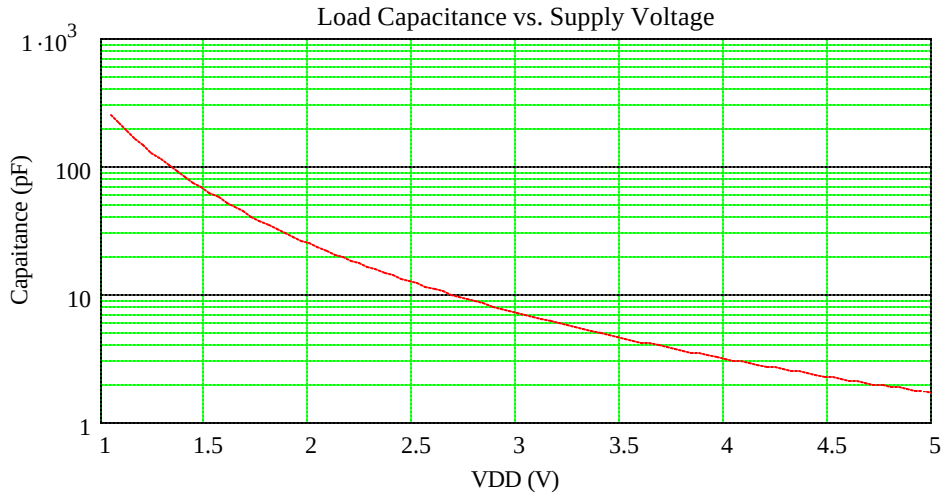
$V_{DD_i} := \frac{i}{num} \cdot (4V) + 1V$

$$C_i := \frac{16 \cdot k \cdot Temp}{\left(V_{DD_i} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSopt}\left(V_{DD_i}\right)\right)^2} \cdot \left(1 + 3 \cdot \frac{V_{DSsati}}{V_{DSopt}\left(V_{DD_i}\right)}\right) \cdot 10^{\frac{SNR}{10}}$$

You will see many different calculations of optimal V_{DSsat}. Consistently for most circuits the value is very close to $V_{DD}/10$, so this may be used as general rule of thumb in non-critical applications

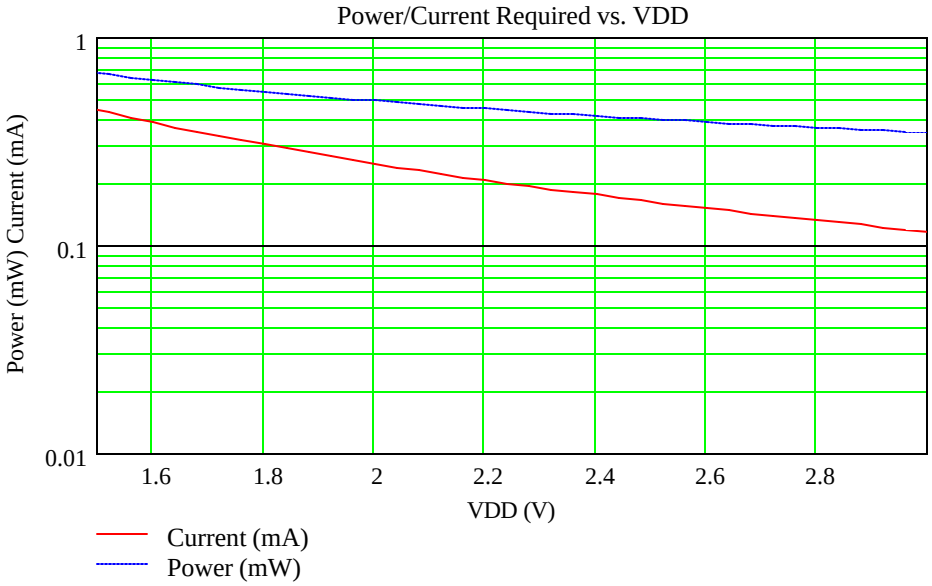


For low supply voltages, the required load capacitance increases rapidly. For every reduction in swing by a factor of two, the load capacitance must increase by a factor of 4 to maintain SNR with the lower swing. For very small supply voltages, the V_{DSsat}s of the output may become a bigger portion of the output swing, increasing the capacitance requirements further.



This indicates caution for using low supply voltages for high performance analog circuits. The following figure will show the power changes slowly with V_{DD}, even though the current changes quickly. This power savings can be lost if the a linear regulator is used to generate the supply voltage from the battery. Also note that even if the power changes slowly with V_{DD}, the required capacitance (and thus die area) changes rapidly with supply voltage. The following figure plots the required current and power dissipation vs. supply voltage.

$$I_i := 4 \cdot f_s \cdot C_i \cdot \left(V_{DD_i} - 2 \cdot V_{DSsatcas} - 2 \cdot V_{DSopt}\left(V_{DD_i}\right) \right)$$



Outputs

$V_{DSopt}(2.7V) = 0.3\,V$ Optimal V_{DSsat} for min. power

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